Electronic Component Zero Orientation For CAD Library Construction









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1 INTRODUCTION

1.1 Scope

To establish a consistent technique for the description of electronic component orientation, and their land pattern geometries, that facilitates and encourages a common data capture and transfer methodology amongst and between global trading partners.

1.2 Purpose

IPC, in conjunction with the International Electrotechnical Commission (IEC), have established several standards that are in the process of being coordinated. One of the standards is on the design of land patterns geometries (IPC-7351/IEC 61188-5-1); the other set is on electronic description for data transfer between design and manufacturing (IPC-2581/IEC 61182-2). In order to maintain a consistent method where these two important standards describe the component mechanical outlines, and their respective mounting platforms, a single concept must be developed that takes into account various factors within the global community.

One of these factors is that of establishing a CAD component description and land pattern standard that adopts a fixed Zero Component Orientation so that all CAD images are built with the same rotation for the purpose of assembly machine automation.

The land pattern standards clearly define all the properties necessary for standardization and acceptability of a "One World CAD Library". The main objective in defining a one world CAD library is to achieve the highest level of "Electronic Product Development Automation". This encompasses all the processes involved from engineering to PCB layout to fabrication, assembly and test. The data format standards need this type of consistency in order to meet the efficiency that electronic data transfer can bring to the industry.

Many large firms have spent millions of dollars creating and implementing their own unique standards for their own "Electronic Product Development Automation". These standards are proprietary to each firm and are not openly shared with the rest of the industry. This has resulted in massive duplication of effort costing the industry millions of man hours in waste and creating industry chaos and global non-standardization.

The industry associations responsible for component descriptions and tape and reel orientation have tried valiantly to influence the industry by making good standards that describe the component outlines and how they should be positioned in the delivery system to the equipment on the manufacturing floor (Appendix A). Suppliers of parts have either not adhered to the recommendations or have misunderstood the intent and provided their products in different orientations. (Appendix B).

The Land pattern standards (both IPC-7351 and IEC 61188-5-1) put an end to the "Proprietary Intellectual Property" and introduce a world standard so every electronics firm can benefit from Electronic Product Development Automation. The data format standards (IPC-2581 and IEC 61182-2) are an open database XML software code that is neutral to all the various CAD ASCII formats. For true machine automation to exist, the world desperately needs a neutral CAD database format that all PCB manufacturing machines can read.

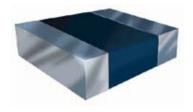
The main purpose of creating the land pattern standards is to achieve reliable solder joint formation platforms; the reason for developing the data transfer structure is to improve the efficiency with which engineering intelligence is converted to manufacturing reality. Even if the neutral CAD format can drive all the manufacturing machines, it would be meaningless unless the component description standard for CAD land patterns was implemented with some consistency. Zero Component Orientation has a key role in machine automation.

The obvious choice for global standardization for EE hardware engineering, PCB design layout, manufacturing, assembly and testing processes is to incorporate the standard land pattern conventions. Any other option continues the confusion and additional manual hours of intervention in order to achieve the goals of automation. In addition, the ease of having one system export a file so that another system can accomplish the work may require unnecessary manipulation of the neutral format in order to meet the object of clear, unambiguous software code.

The design of any assembly will continue to permit arrangement and orientation of components at any orientation consistent with design standards. Starting from a commonly understood data capture concept will benefit the entire supply chain.

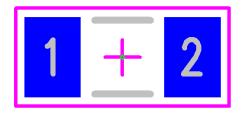
2 CHIP COMPONENTS

2.1 Chip Capacitor



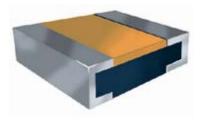
Component

Pin 1 on Left Side



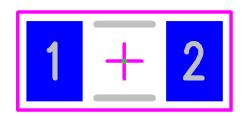
Land Pattern

2.2 Chip Resistor



Component

Pin 1 on Left Side



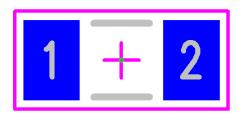
Land Pattern

2.3 Chip Inductor



Component

Pin 1 on Left Side



Land Pattern

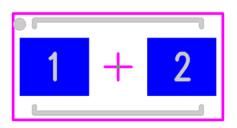
3 MOLDED COMPONENTS

3.1 Molded Capacitors



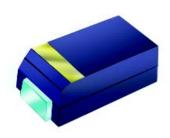
Component

Pin 1 on Left Side



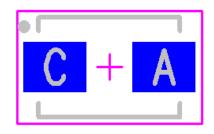
Land Pattern

3.2 Molded Diodes



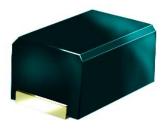
Component

Pin 1 on Left Side (Cathode)



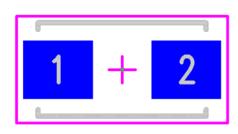
Land Pattern

3.3 Molded Inductors



Component

Pin 1 on Left Side



Land Pattern

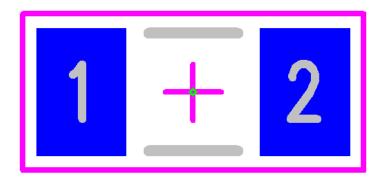
4 PRECSION WIRE-WOUND

4.1 Precision Wire Wound Components



Component

Pin 1 on Left Side



Land Pattern

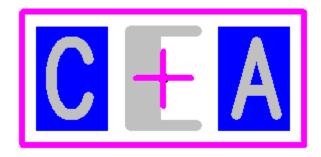
5 MELF COMPONENTS

5.1 MELF Diodes



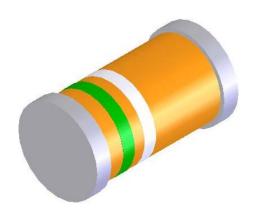
Component

Pin 1 on Left Side (Cathode)



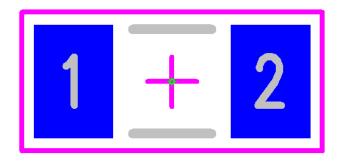
Land Pattern

5.2 MELF Resistors



Component

Pin 1 on Left Side

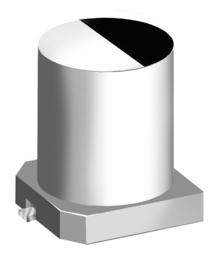


Land Pattern

Note: Pin 1 is always the "Polarity Mark" pin or Cathode

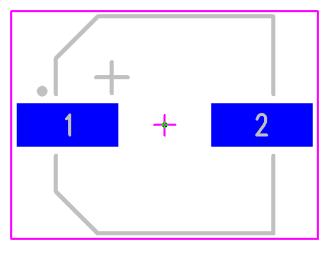
6 ALUMINUM ELECTROLYTIC CAPACITORS

6.1 Aluminum Electrolytic Capacitors



Component

Pin 1 on Left Side



Land Pattern

7 SOT COMPONENTS

7.1 SOT23-3



Component

7.2 SOT23-5



Component

7.3 SOT343



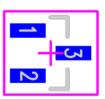
Component

7.4 SOT223



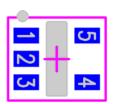
Component

Pin 1 on Upper Left



Land Pattern

Pin 1 on Upper Left



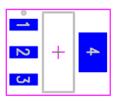
Land Pattern

Pin 1 on Upper Left



Land Pattern

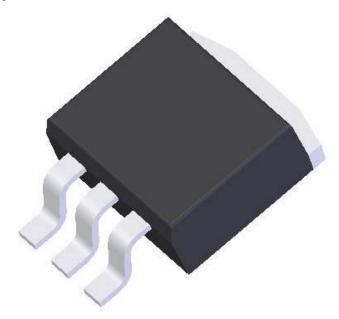
Pin 1 on Upper Left



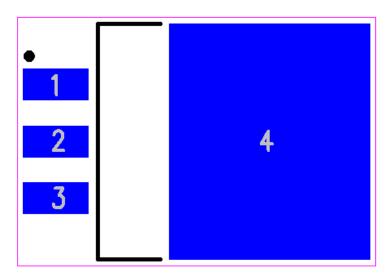
Land Pattern

8 TO COMPONENTS

8.1 TO252 (DPAK)



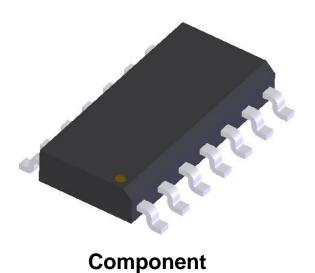
Component



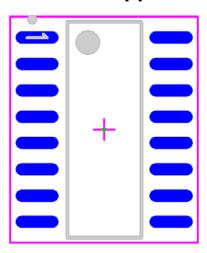
Land Pattern

9 SMALL OUTLINE GULLWING COMPONENT

9.1 SOIC, SOP & SSOP



Pin 1 on Upper Left



Land Pattern

9.2 TSSOP



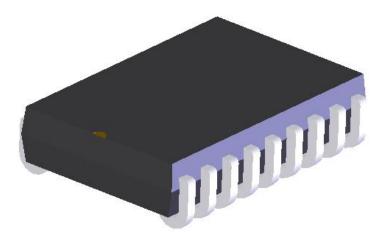
Component



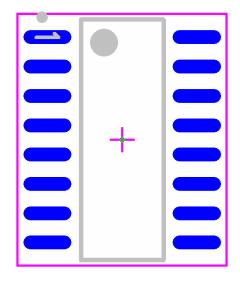
Land Pattern

10 SMALL OUTLINE J-LEAD COMPONENTS

10.1 SOIC J-Lead



Component



Land Pattern

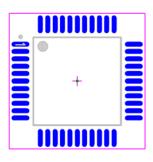
11 QUAD FLAT PACKAGE

11.1 Square QFP Pin 1 on Side



Component

Pin 1 on Upper Left



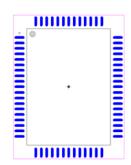
Land Pattern

11.2 Rectangle QFP Pin 1 on Side



Component

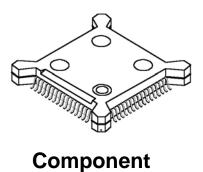
Pin 1 on Upper Left



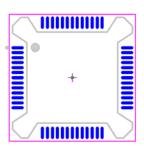
Land Pattern

12 BUMPER QUAD FLAT PACKAGE

12.1 Bump QFP Pin 1 on Side



Pin 1 on Upper Left



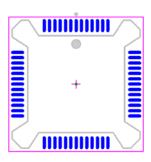
Land Pattern

12.2 Bump QFP Pin 1 in Center



Component

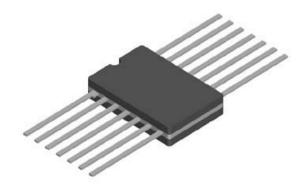
Pin 1 on Top Center



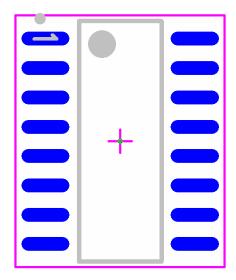
Land Pattern

13 CERAMIC FLAT PACKAGE

13.1 Ceramic Flat Package



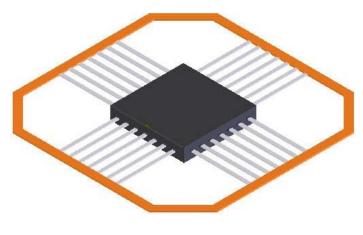
Component



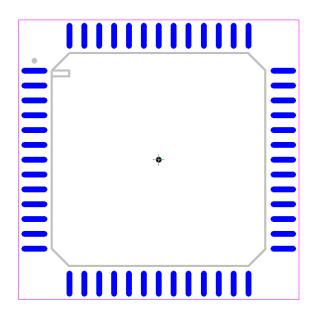
Land Pattern

14 CERAMIC QUAD FLAT PACKAGE

14.1 CQFP (Ceramic Quad Flat Package)



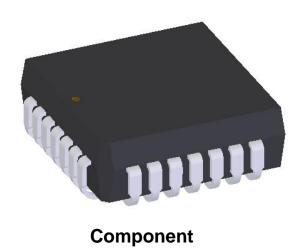
Component



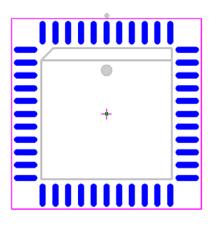
Land Pattern

15 PLASTIC LEADED CHIP CARRIERS

15.1 PLCC Square

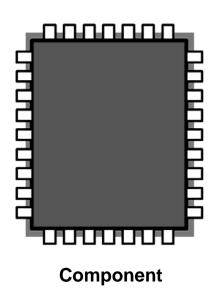


Pin 1 on Top Center

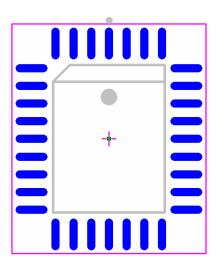


Land Pattern

15.2 PLCC Rectangular



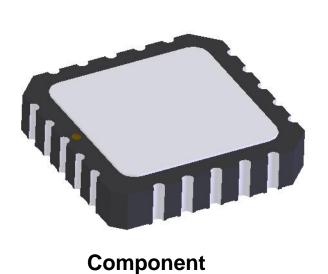
Pin 1 on Top Center



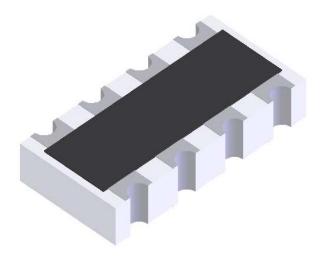
Land Pattern

16 LEADLESS CHIP CARRIERS

16.1 LCC Square

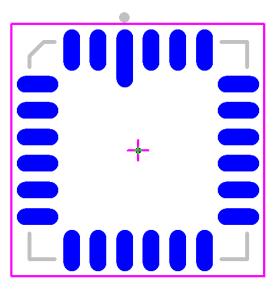






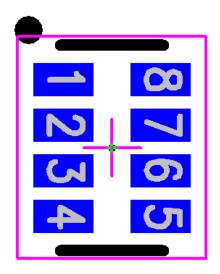
Component

Pin 1 on Top Center



Land Pattern

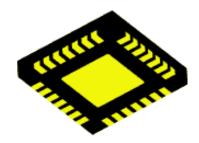
Pin 1 on Upper Left



Land Pattern

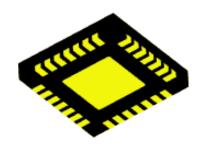
17 QUAD FLAT NO-LEAD

17.1 QFN Square



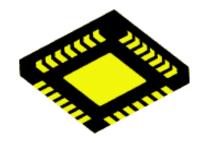
Component (Bottom View)

17.2 QFN Rectangular Vertical



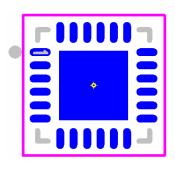
Component (Bottom View)

17.3 QFN Rectangular Horizontal



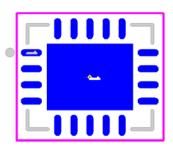
Component (Bottom View)

Pin 1 on Upper Left



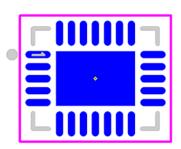
Land Pattern

Pin 1 on Upper Left



Land Pattern

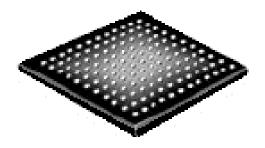
Pin 1 on Upper Left



Land Pattern

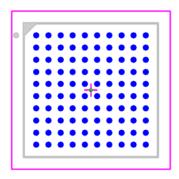
18 BALL GRID ARRAY

18.1 BGA Square



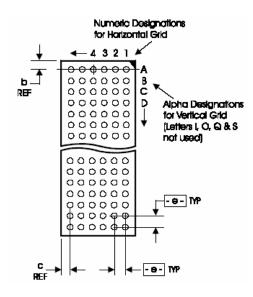
Component (Bottom View)

Pin A1 in Upper Left



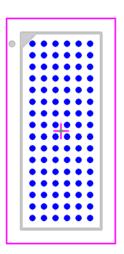
Land Pattern

18.2 BGA Rectangular



Component (Bottom View)

Pin A1 in Upper Left



Land Pattern

19 COMPONENT ZERO ORIENTATIONS

19.1 Summary

Surface Mount Land Patterns

IPC-735* Component Family Breakdown:

```
IPC-7351 = IEC 61188-5-1, Generic requirements - land/joint considerations - General Description

IPC-7352 = IEC 61188-5-2, Sectional requirements - land/joint considerations - Discrete Components

IPC-7353 = IEC 61188-5-3, Sectional requirements - land/joint considerations - Gull-wing leads, two sides (SOP)

IPC-7354 = IEC 61188-5-4, Sectional requirements - land/joint considerations - J leads, two sides (SOJ)

IPC-7355 = IEC 61188-5-5, Sectional requirements - land/joint considerations - Gull-wing leads, four sides (QFP)

IPC-7356 = IEC 61188-5-6, Sectional requirements - land/joint considerations - J leads, four sides (PLCC)

IPC-7357 = IEC 61188-5-7, Sectional requirements - land/joint considerations - Post leads, two sides (DIP)

IPC-7358 = IEC 61188-5-8, Sectional requirements - land/joint considerations - Area Array Components (BGA)

IPC-7359 = NO IEC Document, Sectional requirements - land/joint considerations - No Lead Components (LCC)
```

Component Zero Orientations Pin 1 Location For CAD Library Construction

- 1) Chip Capacitors, Resistors and Inductors (RES, CAP and IND) Pin 1 (Positive Pin) on Left
- 2) Molded Inductors (INDM), Resistors (RESM) and Tantalum Capacitors (CAPT) Pin 1 (Positive Pin) on Left
- 3) Precision Wire-wound Inductors (INDP) Pin 1 (Positive Pin) on Left
- 4) MELF Diodes Pin 1 (Cathode) on Left
- 5) Aluminum Electrolytic Capacitors (CAPAE) Pin 1 (Positive) on Left
- 6) SOT Devices (SOT23, SOT23-5, SOT223, SOT89, SOT143, etc.) Pin 1 Upper Left
- 7) TO252 & TO263 (DPAK Type) Devices Pin 1 Upper Left
- 8) Small Outline Gullwing ICs (SOIC, SOP, TSOP, SSOP, TSSOP) Pin 1 Upper Left
- 9) Ceramic Flat Packs (CFP) Pin 1 Upper Left
- 10) Small Outline J Lead ICs (SOJ) Pin 1 Upper Left
- 11) Quad Flat Pack ICs (PQFP, SQFP) Pin 1 Upper Left
- 12) Ceramic Quad Flat Packs (CQFP) Pin 1 Upper Left
- 13) Bumper Quad Flat Pack ICs (BQFP Pin 1 Center) Pin 1 Top Center
- 14) Plastic Leaded Chip Carriers (PLCC) Pin 1 Top Center
- 15) Leadless Chip Carriers (LCC) Pin 1 Top Center
- 16) Chip Array Pin 1 Upper Left
- 17) Quad Flat No-Lead ICs (QFN) QFNS, QFNRV, QFNRH Pin 1 Upper Left
- 18) Ball Grid Arrays (BGA) Pin A1 Upper Left

20 APPENDIX A - EIA Survey for Component Orientation

Date: 04 February 2003

TO:

END USERS AND SUPPLIERS OF COMPONENT PACKAGES SUPPLIED ON TAPE

FROM:

ELECTRONIC INDUSTRIES ALLIANCE (EIA)
AUTOMATED COMPONENT HANDLING COMMITTEE (ACH)

SUBJECT:

EIA SURVEY FOR ORIENTATION OF COMPONENTS SUPPLIED ON TAPE

SPECIFICALLY:

STANDARD EIA-481-B, "8 mm through 200 mm Embossed Carrier

Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling".

CAUTION: THE INDUSTRY STANDARD MAY CHANGE! WE REQUEST YOUR COMMENTS.

20.1 Purpose

The Automated Component Handling Committee develops and maintains industry engineering standards and publications for tape, reels, magazines, trays, etc. for handling components in production. It also provides technical input to US national positions on related international standards issues and proposals. Based on a number of industry queries, the committee has decided to survey industry to determine the need for an improved standard for orientation of component packages in tape and reel.

Pending the outcome of this survey, a change proposal to the EIA-481B standard will be prepared and presented for approval during 2003. This is your opportunity to have your comments considered.

Please complete the survey attached to the e-mail as the file entitled, "Part 2" by 15 March 2003 and email the completed survey to the following address: engineering@ecaus.org

20.2 Driving factors

The following areas in EIA 481B can still cause confusion as to orientation: Factor 1 (F1):

Ambiguity exists on how to interpret terminology such as 'Termination #1' and 'SOT23-5' Factor 2 (F2):

Inconsistency exists on how components that share a common outline are oriented in tape; for example, a 'SOT223' and a 'SOT89' are supplied in tape with orientations that do not match.

These factors result in ambiguity during the taping process for the supplier. These factors may also result in components that are supplied in orientations that are not acceptable for automating the component pick-and-place process for the end user. EIA-481B, Section 4.14 documents the current standard for determining component package orientation in tape.

20.3 Examples of Possible Conflict

Driving factor F1 is illustrated by applying the current standard to a 5 termination 'SOT23' package (Figure 1a and 1b). The examples show that the same component package may have three different orientations in tape based on different package outline names as well as non standardized termination numbering conventions by various component manufacturers. Inconsistent orientation in tape for the same component creates an unacceptable condition for automating the component pick-and-place process.

Drawing Pkg Outline Name EIA-481B rule used Orientation in tape As found on website datasheet After applying EIA-481B rule Termination designation as shown Based on package name If called a 'SOT23' then apply EIA-481B, 4.14.q (Termination #1 in SOT23, 5L 1 2 Quadrant 3) 5/SOT23 2 SOT23-5 If not called 'SOT23', JEDEC: MO-178 then apply EIA-481B, 4.14.e, 4.14.f (Long axis perpendicular to feed, Termination#1 toward round holes) 2

Figure 1a: Internal Part number 'X', Approved Manufacturer 'A'

Figure 1b: Internal Part number 'X', Approved Manufacturer 'B'

Drawing	Pkg Outline Name	EIA-481B rule used	Orientation in tape
3 4 5	As found on website datasheet As found on website datasheet Mini5-G1 Package EIAJ: SC-74A	If called a 'SOT23' then apply EIA-481B, 4.14.g (Termination #1 in Quadrant 3)	After applying EIA-481B rule 3 4 5
		If not called 'SOT23', then apply EIA-481B, 4.14.e, 4.14.f (Long axis perpendicular to feed, Termination#1 toward round holes)	 1 2

Driving factor F2 is illustrated by applying the current standard to a SOT223 and SOT89 package (Figure 2). The example shows that packages that share similar geometric attributes have two different orientations in tape. Pick-and-place equipment machine recognition systems identify component packages by the arrangement of terminations on the package body. Component packages with similar outlines should share the same orientation in tape to minimize possibility of confusion between the packages.

Drawing Termination designation as shown	Pkg Outline Name As found on website datasheet	EIA-481B rule used Based on package name	Orientation in tape After applying EIA-481B rule
1 2 3	SOT223 JEDEC: TO-261 EIAJ: SC-73	If called a 'SOT223' then apply EIA-481B, 4.14.g (Termination #1 in Quadrant 3)	0 4 3 3 2 2 1 1 1
1 2 3	SOT89 JEDEC: TO-293	If not called 'SOT89', then apply EIA-481B, 4.14.g (Termination#1 in Quadrant 4)	3 2 1 0 4

Figure 2: Current standard applied to SOT223 and SOT89 packages

20.4 Recommendation

To address the issues described in the driving factors, the following orientation rules shall be considered as standard for multi-connection components.

- 1. Traditionally packaged components with leaded, bottom-only terminations (e.g. PLCC, SOIC, SOJ, and BGA) shall be packaged with the terminations facing the bottom of the carrier cavity. The following rules apply whether the terminations are facing downward or upward in the cavity.
- 2. Termination is the electrical or mechanical connection from the component to the board and can be described as lead, pin, bump, ball, wire-pad, connector, etc.
- 3. Orienting feature is the attribute on the component that identifies a unique orientation and can be described as fiducial mark, chamfered edge, dimple, notch, wider termination, etc. If the orienting feature is located in the exact center of the component, or it lies on the shorter axis of the component, then an alternate orienting feature on the component should be chosen.
- 4. A component is described as square if the bounding rectangle around the outer extents of the component, (including body and terminations) contains edges with equal lengths; i.e. A = B
- 5. The tape pocket quadrant designations that describe the taped orientation of components are shown Figure 3.
- 6. Use the rules in the sequence shown in the following flow chart (Figure 4) to determine the correct orientation of the component in the tape pocket.

7. The rules described in this standard shall supersede all prior standards established in EIA-481 EIA-800 for the following component packages: SOT23, SOT143, SOT89, SOT223, IPD.

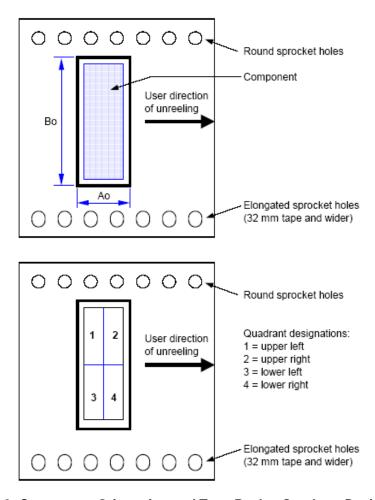


Figure 3: Component Orientation and Tape Pocket Quadrant Designations

Outline Name	Reference JEDEC (EIAJ)	Drawing	Current	Recommended
SOT23	TO236			
S0T143	TO-253			
S0T23-5	MO-178			
S0T223	TO-261 (SC-73)			
SOT89	T0-243			
DPAK	TO-252 (SC-63)			

Figure 4: Summary of new rules applied to common component packages (1 of 2)

Outline Name	Reference JEDEC (EIAJ)	Drawing	Current	Recommended
PLCC28	MS-018	MSC645	00000	00000
S08	MS-012	MSD406	00000	00000
QFP44			00000	00000
BGA		MODIFIE		00000

Figure 5: Summary of new rules applied to common component packages (2 of 2)

Notice:

Copies of the **current version of the EIA-481-B** standard are available for purchase via the Internet from EIA's publications distributor; Global Engineering Documents at: http://global.ihs.com by typing in EIA481 in the "Document Number" block as shown and then clicking the "Search" block.

20.5 Presentation of Results

Edward F. Mikoski, Jr. Spring 2003 (Excerpts)

Component Manufacturer (on orientation issues)

- Our customer base has conflicting perceptions as to how the orientation standard is understood.
- Based upon its wording today, we have little leverage to request orientation consistency.
- Wholesale changes will be difficult and cost prohibitive. However, all new packages and tooling releases should follow the proposed changes.

End User (on the proposed new rules)

- This would require us to overhaul our test handlers to accommodate a 90 degree rotation of the device.
- The cost involved in a project such as this would be more than we plan to budget for the test equipment.
- To upgrade, the equipment will need a new or modified feeder system, orientation station and Pick and Place head design.
- Modifications will need to be made to the vision inspection systems allowing inspection of the part at the proposed orientation.

EMS

• Under new rules the machine operator will have to reprogram orientation of existing products.

End User (on other issues that the committee should address)

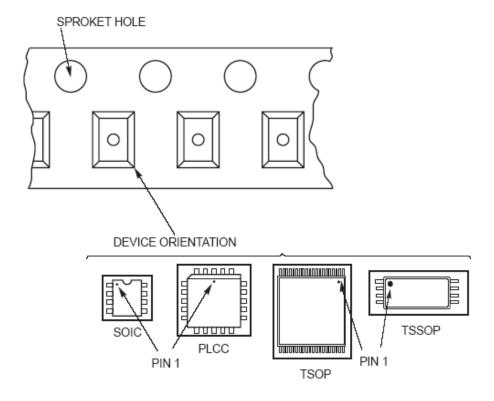
- 1. Adopting the Cartesian coordinate system for identifying quadrants.
- 2. Addressing of bare die orientation in tape.
- 3. Addressing of component orientation in matrix trays as illustrated by example methodology used in the EIA Orientation Survey.

General Comment Received

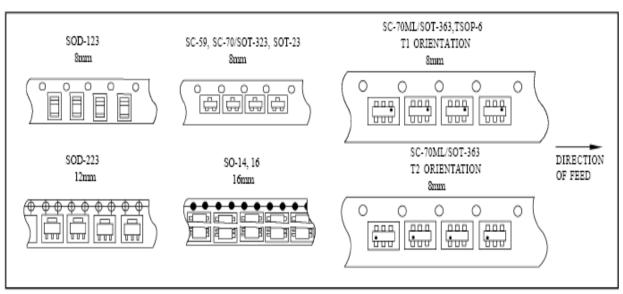
The proposal deviates for many packages from what is currently used. We feel that
inconsistencies remain even with the new standard since the "old" orientations will remain on the
market. Hence, we will have more inconsistencies in the future. To overcome that we propose
that there should be at least a joint JEITA - EIA standard.

21 APPENDIX B – Internet Search Results

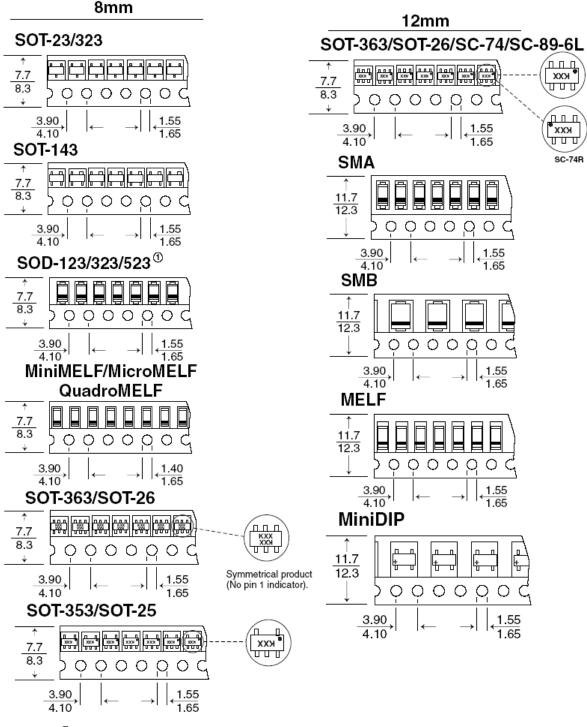
21.1 Device Orientation (Catalyst)



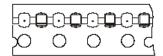
21.2 Device Orientation (LRC China)



21.3 Device Orientation (Diodes, Incorporated)

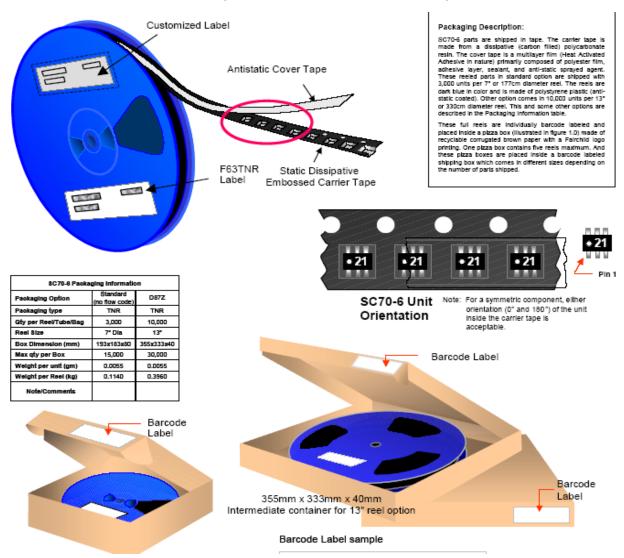


SOD-523 has alternating empty cavities as indicated below.



Direction of unreeling

21.4 Device Orientation (Fairchild Semiconductor)

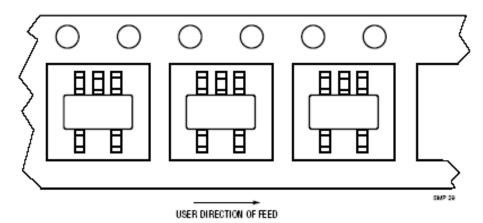


21.5 Device Orientation (Linear Technology)

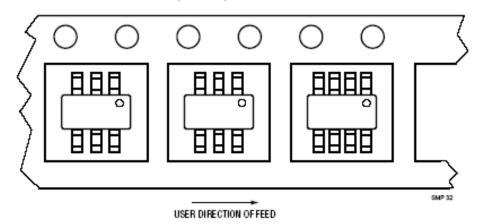
S3
SOT-23 Devices

USER DIRECTION OF FEED

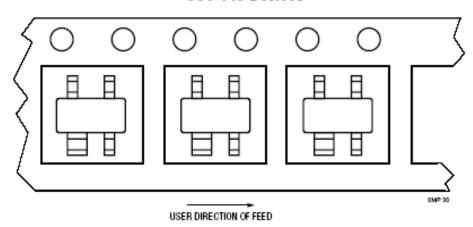
S5 TSOT, SOT-23 Devices



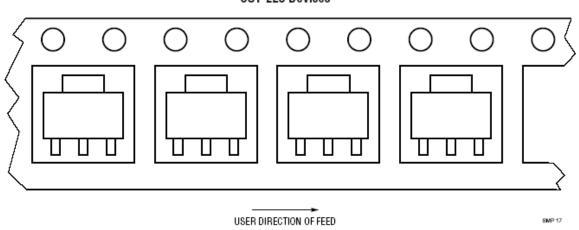
SC6, S6 and TS8 SC70, TSOT, SOT-23 Devices



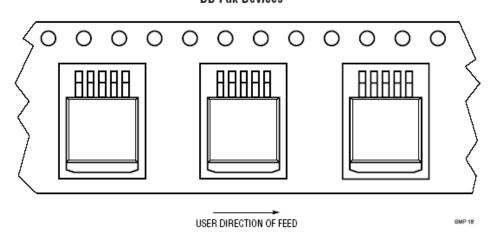
S4 SOT-143 Devices



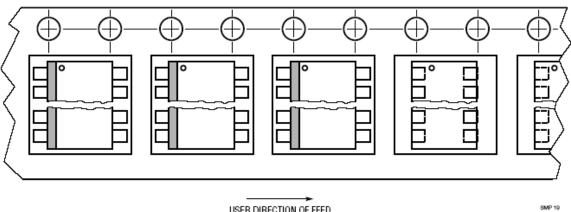
ST SOT-223 Devices



M, Q, R **DD Pak Devices**

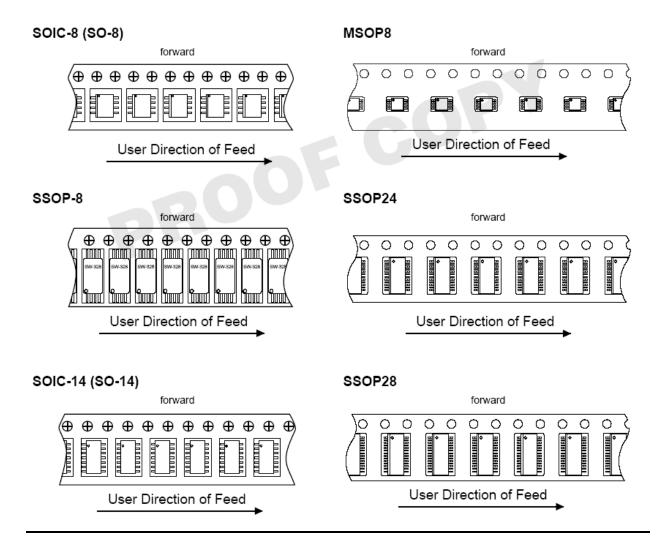


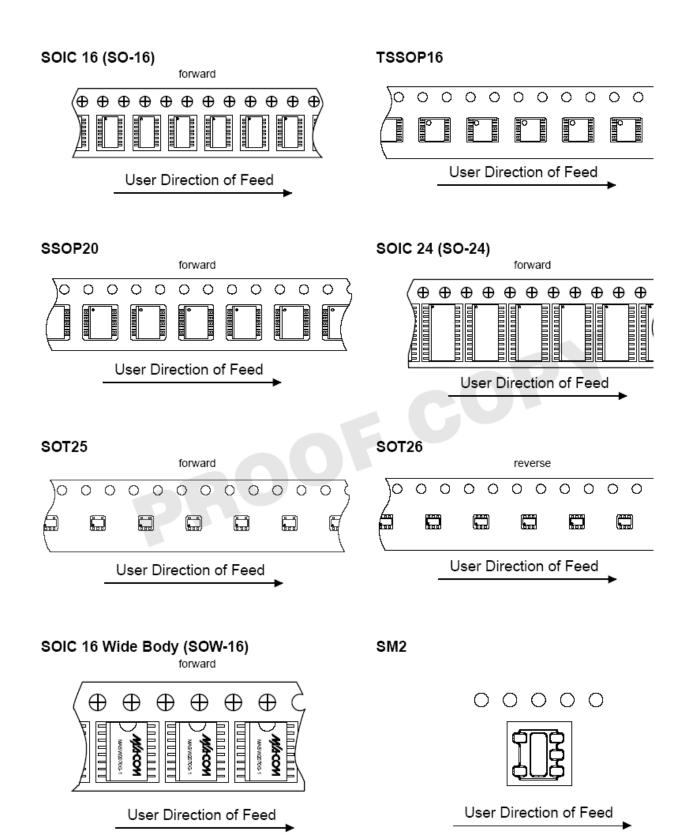
DD, DE, F, FE, FW, G, GN, GW, S8, S, SW, MS8, MS, MS8E, MSE, SSOP, TSSOP, UD, UE, UF and UH Devices



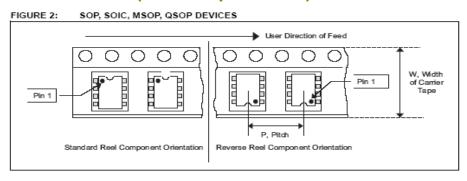
USER DIRECTION OF FEED

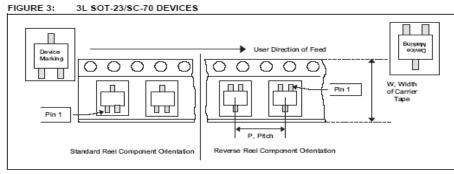
21.6 Device Orientation (RF Technologies)

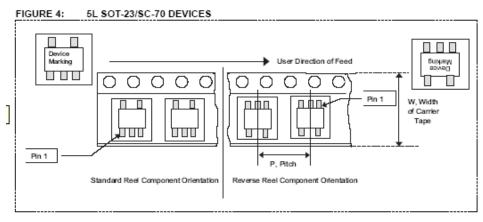


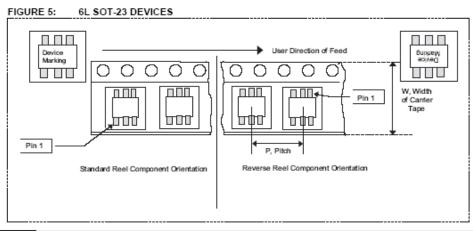


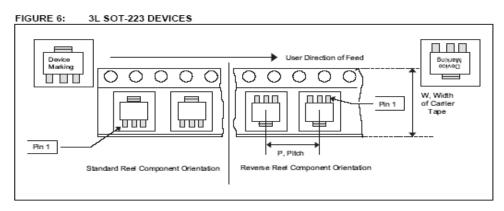
21.7 Device Orientation (Microchip Devices)

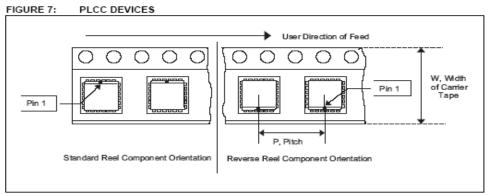


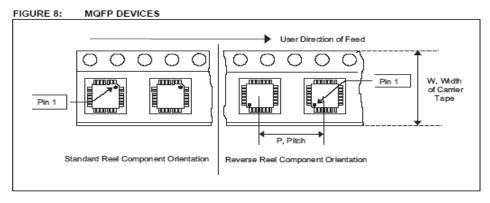












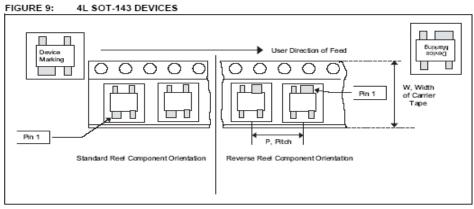


FIGURE 10: 3L/5L/7L DDPAK AND 3L DPAK DEVICES

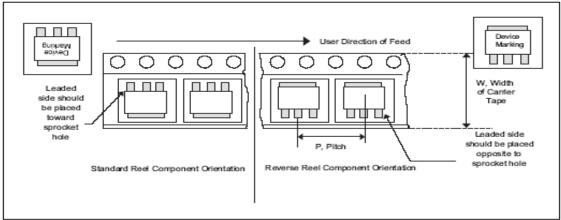


FIGURE 11: SOT-89 DEVICES

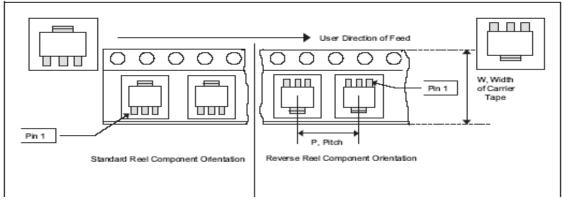
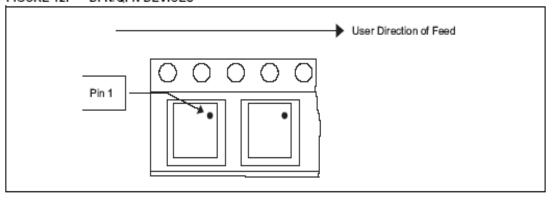


FIGURE 12: DFN/QFN DEVICES



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P. Pitch Device Marking 3 LEAD TO-92 W, Width of Carrier Tape Device Marking 2 LEAD TO-92 W, Width of Carrier Tape Reverse Reel Component Orientation Component Orientation H₁

FIGURE 13: TO-92 DEVICES

DIMENSIONS AND TOLERANCES

All component taping diagrams, dimensions, tolerances, and component positioning requirements are those which are specified per EIA Standard EIA-481, current revision.

For the 8-lead SOIC EIAJ Type II Package and 16 mm Carrier Tape width, the component taping diagrams, dimensions, and tolerances, and component positioning requirements are those which are specified per EIAJ Standard RC-1009B, current revision.

21.8 Device Orientation (ZETEX)

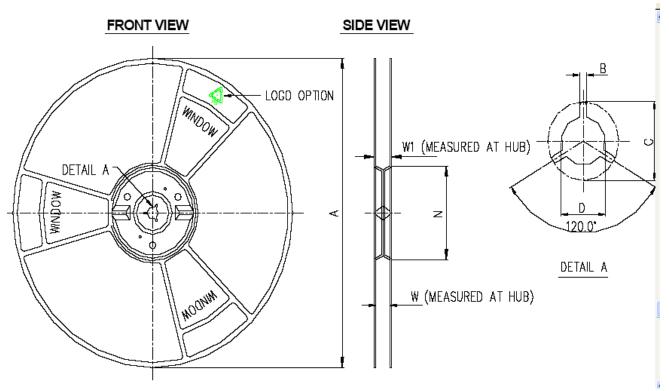


COMPONENT ORIENTATION

In all cases the device mounting side is orientated to the bottom side of the component compartment. This being the tape side which cannot be seen during unreeling.

Package	Orientation Diagrams	Tape Width (mm)	Reel Size Supplied	No. Of Components	Tape Option Indicator
SOT223		12 12	7" (180mm) 13" (330mm)	1,000 4,000	TA TC
SOT89		12	7" (180mm)	1,000	TA
SOT23	\(\)	8 8	7" (180mm) 13" (330mm)	3,000 10,000	TA TC
SM8	Pin 1	12 12	7" (180mm) 13" (330mm)	1,000 4,000	TA TC
* SO8 QSOP14 QSOP16	Paul	12 12	7" (180mm) 13" (330mm)	500 2500	TA TC
x S016 QS0P20/24/28		16 16	7" (180mm) 13" (330mm)	500 2500	TA TC

21.9 Device Orientation (IDT)

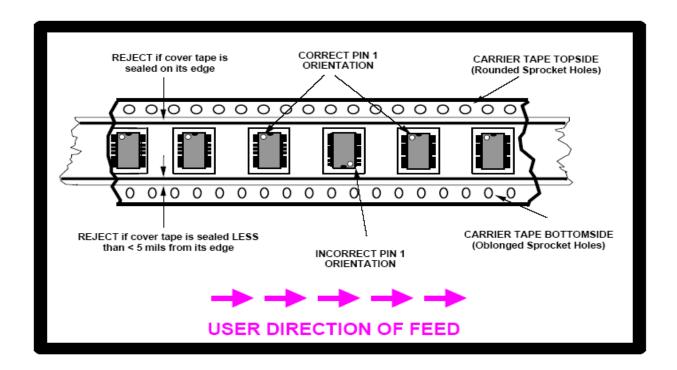


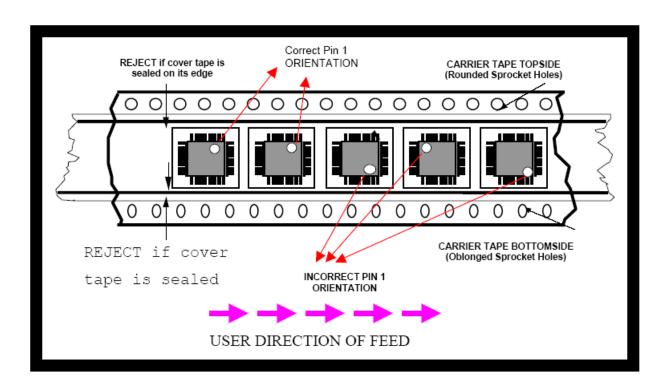


Tape and Reel

General Information

The Tape and Reel packaging materials shall not adversely affect the visual, mechanical, and electrical characteristics or markings of the components. In all cases, the components must be protected from bent leads, lead contamination, ESD damage, and any matter that may interfere with the soldering or normal use of the product. All Tape and Reel materials were formulated to provide dimensions and tolerances necessary to tape surface mount components such that they may be automatically handled. Tape and Reel materials meet EIA-481-B requirements for embossed carrier taping of surface mount components for automatic handling, including IDT's standard aging and drop tests.





22 APPENDIX C - Comment Form

The purpose of this form is to provide the Technical Committees of IPC and the IEC with input from the industry regarding usage of the subject of Zero Component Orientation Recommendations.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC-Association Connecting Electronics Industries 3000 Lakside Drive Suite 309S Bannockburn, IL, 60015 Tel: 847-615-7100 Fax: 847-615-7105

Web: www.ipc.org Email: answers@ipc.org

1. I recommend changes to the following:		
Requirement		
Paragraph number		
Other		
Recommendations for correction:		
3. Other suggestions for document improve		
Submitted by:		
Name	Telephone	
Company	E-mail	
Address		
City/State/Zipcode		
Date:		

23 CREDITS

23.1 Contributions

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