TEXAS INSTRUMENTS
www.ti.com

LMV341, LMV342, LMV344
RAIL-TO-RAIL OUTPUT CMOS OPERATIONAL AMPLIFIERS WITH SHUTDOWN

SLOS447G – SEPTEMBER 2004 – REVISED FEBRUARY 2006

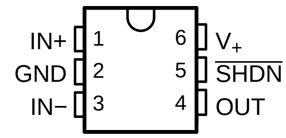
FEATURES

- **2.7-V and 5-V Performance**
- **Rail-to-Rail Output Swing**
- **Input Bias Current**…**1 pA Typ**
- **Input Offset Voltage**…**0.25 mV Typ**
- **Low Supply Current**…**100 μA Typ**
- **Low Shutdown Current**…**45 pA Typ**
- **Gain Bandwidth of 1 MHz Typ**
- **Slew Rate**…**1 V/μs Typ**
- **Turn-On Time From Shutdown**…**5 μs Typ**
- **Input Referred Voltage Noise (at 10 kHz)**… **20 nV/√Hz**
- **ESD Protection Exceeds JESD 22**
  - **– 2000-V Human-Body Model (A114-A)**
  - **– 200-V Machine Model (A115-A)**

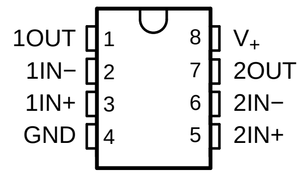
APPLICATIONS

- **Cordless/Cellular Phones**
- **Consumer Electronics (Laptops, PDAs)**
- **Audio Pre-Amps for Voice**
- **Portable/Battery-Powered Electronic Equipment**
- **Supply-Current Monitoring**
- **Battery Monitoring**
- **Buffers**
- **Filters**
- **Drivers**

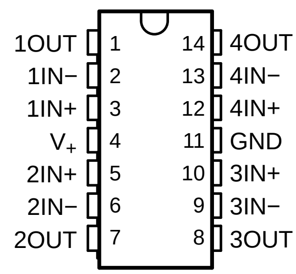
LMV341 . . . DBV (SOT-23) OR DCK (SC-70) PACKAGE
(TOP VIEW)



LMV342 . . . D (SOIC) OR DGK (MSOP) PACKAGE
(TOP VIEW)



LMV344 . . . D (SOIC) OR PW (TSSOP) PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The LMV341, LMV342, LMV344 devices are single, dual, and quad CMOS operational amplifiers, respectively, with low voltage, low power, and rail-to-rail output swing capabilities. The PMOS input stage offers an ultra-low input bias current of 1 pA (typ) and an offset voltage of 0.25 mV (typ). The single supply amplifier is designed specifically for low-voltage (2.7 V to 5 V) operation, with a wide common-mode input voltage range that typically extends from –0.2 V to 0.8 V from the positive supply rail. The LMV341 (single) also offers a shutdown ($\overline{\text{SHDN}}$) pin that can be used to disable the device. In shutdown mode, the supply current is reduced to 33 nA (typ). Additional features of the family are a 20-nV/√Hz voltage noise at 10 kHz, 1-MHz unity-gain bandwidth, 1-V/μs slew rate, and 100-μA current consumption per channel.

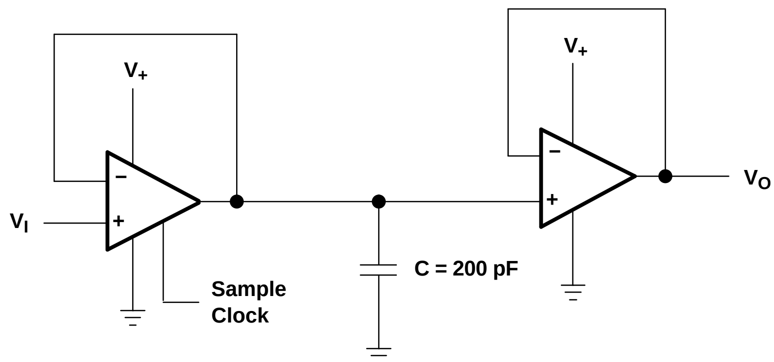
Offered in both the SOT-23 and smaller SC-70 packages, the LMV341 is suitable for the most space-constraint applications. The LMV342 dual device is offered in the standard SOIC and MSOP packages. An extended industrial temperature range from –40°C to 125°C makes these devices suitable in a wide variety of commercial and industrial environments.

ORDERING INFORMATION

T_A	PACKAGE(1)			ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 125°C	Single	SOT-23 – DBV	Reel of 3000	LMV341IDBVR	RC9_
			Reel of 250	LMV341IDBVT	PREVIEW
		SC-70 – DCK	Reel of 3000	LMV341IDCKR	R4_
			Reel of 250	LMV341ICKVT	PREVIEW
	Dual	SOIC – D	Tube of 75	LMV342ID	MV342I
			Reel of 2500	LMV342IDR	
		MSOP/VSSOP – DGK	Reel of 250	LMV342IDGK	RP_
			Reel of 2500	LMV342IDGKR	
	Quad	SOIC – D	Tube of 50	LMV344ID	LMV344I
			Reel of 2500	LMV344IDR	
		TSSOP – PW	Tube of 90	LMV344IPW	MV344I
			Reel of 2000	LMV344IPWR	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK/DGK: The actual top-side marking has one additional character that designates the assembly/test site.

APPLICATION CIRCUIT: SAMPLE-AND-HOLD CIRCUIT



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
V_+	Supply voltage(2)				5.5	V
V_{ID}	Differential input voltage(3)				±5.5	V
V_I	Input voltage range (either input)			0	5.5	V
θ_{JA}	Package thermal impedance(4)(5)	D package	8 pin		97	°C/W
			14 pin		86	
		DBV package			165	
		DCK package			259	
		DGK package			172	
		PW package			113	
T_J	Operating virtual junction temperature				150	°C
T_{stg}	Storage temperature range			–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values (except differential voltages and V_+ specified for the measurement of I_{OS}) are with respect to the network GND.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(5) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions

		MIN	MAX	UNIT
V_+	Supply voltage (single-supply operation)	2.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

ESD Protection

TEST CONDITIONS	TYP	UNIT
Human-Body Model	2000	V
Machine Model	200	V

Electrical Characteristics

$V_+ = 2.7$ V, GND = 0 V, $V_{IC} = V_O = V_+/2$, $R_L > 1$ MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
V_{IO}	Input offset voltage			25°C		0.25	4	mV
				Full range			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.7		μV/°C
I_{IB}	Input bias current			25°C		1	120	pA
				–40°C to 85°C			250	
				–40°C to 125°C			3	nA
I_{IO}	Input offset current			25°C		6.6		fA
CMRR	Common-mode rejection ratio	$0 \le V_{ICR} \le 1.7$ V		25°C	56	80		dB
		$0 \le V_{ICR} \le 1.6$ V		Full range	50			
k_{SVR}	Supply-voltage rejection ratio	$2.7\text{ V} \le V_+ \le 5$ V		25°C	65	82		dB
				Full range	60			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0	–0.2 to 1.9	1.7	V
A_V	Large-signal voltage gain(2)	R_L = 10 kΩ to 1.35 V		25°C	78	113		dB
				Full range	70			
		R_L = 2 kΩ to 1.35 V		25°C	72	103		
				Full range	64			
V_O	Output swing (delta from supply rails)	R_L = 2 kΩ to 1.35 V	Low level	25°C		24	60	mV
				Full range			95	
			High level	25°C		26	60	
				Full range			95	
		R_L = 10 kΩ to 1.35 V	Low level	25°C		5	30	
				Full range			40	
			High level	25°C		5.3	30	
				Full range			40	
I_{CC}	Supply current (per channel)			25°C		100	170	μA
				Full range			230	
I_{OS}	Output short-circuit current	Sourcing	LMV341, LMV342	25°C	20	32		mA
			LMV344		18	24		
		Sinking			15	24		
SR	Slew rate	R_L = 10 kΩ(3)		25°C		1		V/μs
GBM	Unity-gain bandwidth	R_L = 10 kΩ, C_L = 200 pF		25°C		1		MHz
Φ_m	Phase margin	R_L = 100 kΩ		25°C		72		deg
G_m	Gain margin	R_L = 100 kΩ		25°C		20		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		40		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.001		pA/√Hz
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_I = 1 V_{PP}		25°C		0.017		%

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2 V ≤ V_O ≤ V_+ – 0.2 V
(3) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

Shutdown Characteristics

$V_+ = 2.7$ V, GND = 0 V, $V_{IC} = V_O = V_+/2$, $R_L > 1$ MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode	$V_{SD} = 0$ V	25°C		0.045	1000	nA
			Full range			1.5	μA
$t_{(on)}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		1.7 to 2.7	2.4 to 2.7	V
		Shutdown mode			0 to 1	0 to 0.8	

Electrical Characteristics

$V_+ = 5$ V, GND = 0 V, $V_{IC} = V_O = V_+/2$, $R_L > 1$ MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP[1]	MAX	UNIT
V_{IO}	Input offset voltage			25°C		0.25	4	mV
				Full range			4.5	
α_{VIO}	Average temperature coefficient of input offset voltage			Full range		1.9		μV/°C
I_{IB}	Input bias current			25°C		1	200	pA
				–40°C to 85°C			375	
				–40°C to 125°C			5	nA
I_{IO}	Input offset current			25°C		6.6		fA
CMRR	Common-mode rejection ratio	$0 \le V_{ICR} \le 4$ V		25°C	56	86		dB
		$0 \le V_{ICR} \le 3.9$ V		Full range	50			
k_{SVR}	Supply-voltage rejection ratio	$2.7\text{ V} \le V_+ \le 5$ V		25°C	65	82		dB
				Full range	60			
V_{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0	–0.2 to 4.2	4	V
A_V	Large-signal voltage gain[2]	R_L = 10 kΩ to 2.5 V		25°C	78	116		dB
				Full range	70			
		R_L = 2 kΩ to 2.5 V		25°C	72	107		
				Full range	64			
V_O	Output swing (delta from supply rails)	R_L = 2 kΩ to 2.5 V	Low level	25°C		32	60	mV
				Full range			95	
			High level	25°C		34	60	
				Full range			95	
		R_L = 10 kΩ to 2.5 V	Low level	25°C		7	30	
				Full range			40	
			High level	25°C		7	30	
				Full range			40	
I_{CC}	Supply current (per channel)			25°C		107	200	μA
				Full range			260	
I_{OS}	Output short-circuit current	Sourcing	LMV341, LMV342	25°C	85	113		mA
			LMV344		TBD	TBD		
		Sinking			50	75		
SR	Slew rate	R_L = 10 kΩ[3]		25°C		1		V/μs
GBM	Unity-gain bandwidth	R_L = 10 kΩ, C_L = 200 pF		25°C		1		MHz
Φ_m	Phase margin	R_L = 100 kΩ		25°C		70		deg
G_m	Gain margin	R_L = 100 kΩ		25°C		20		dB
V_n	Equivalent input noise voltage	f = 1 kHz		25°C		39		$nV/\sqrt{Hz}$
I_n	Equivalent input noise current	f = 1 kHz		25°C		0.001		$pA/\sqrt{Hz}$
THD	Total harmonic distortion	f = 1 kHz, A_V = 1, R_L = 600 Ω, V_I = 1 V_{PP}		25°C		0.012		%

(1) Typical values represent the most likely parametric norm.
(2) GND + 0.2 V ≤ V_O ≤ V_+ – 0.2 V
(3) Connected as voltage follower with 2-V_{PP} step input. Number specified is the slower of the positive and negative slew rates.

Shutdown Characteristics

$V_+ = 5$ V, GND = 0 V, $V_{IC} = V_O = V_+/2$, $R_L > 1$ MΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{CC(SHDN)}$	Supply current in shutdown mode	$V_{SD} = 0$ V	25°C		0.033	1	μA
			Full range			1.5	
$t_{(on)}$	Amplifier turn-on time		25°C		5		μs
V_{SD}	Shutdown pin voltage range	ON mode	25°C		3.1 to 5	4.5 to 5	V
		Shutdown mode			0 to 1	0 to 0.8	

TYPICAL CHARACTERISTICS

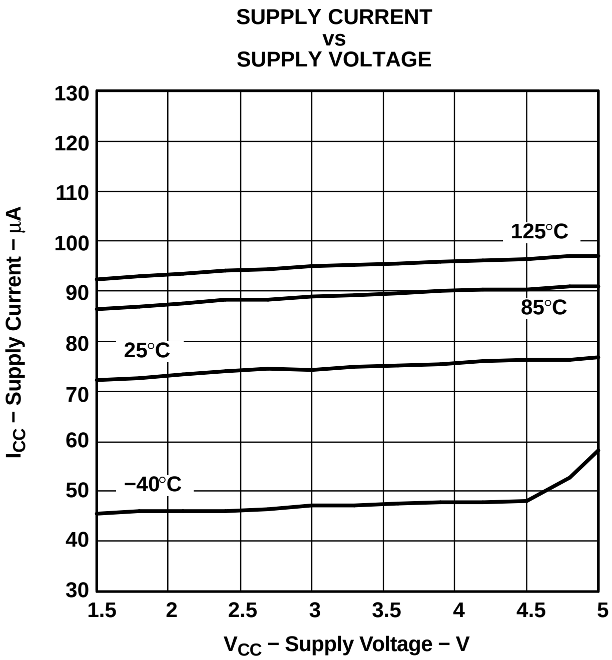


Figure 1.

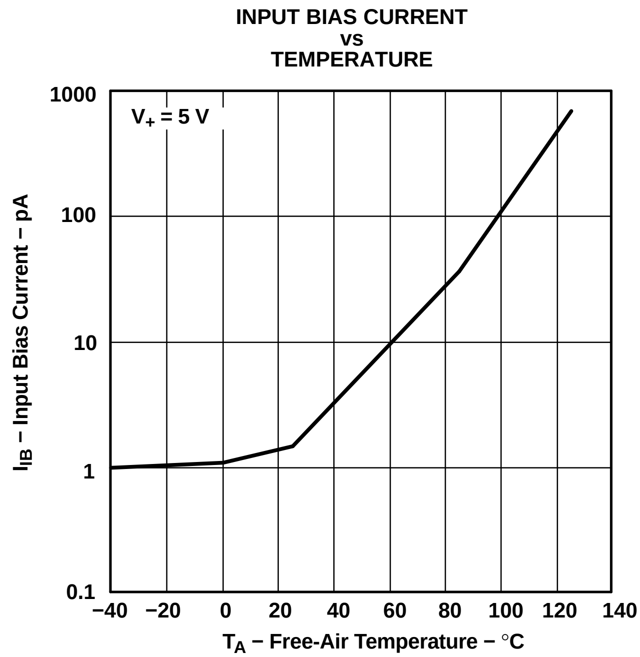


Figure 2.

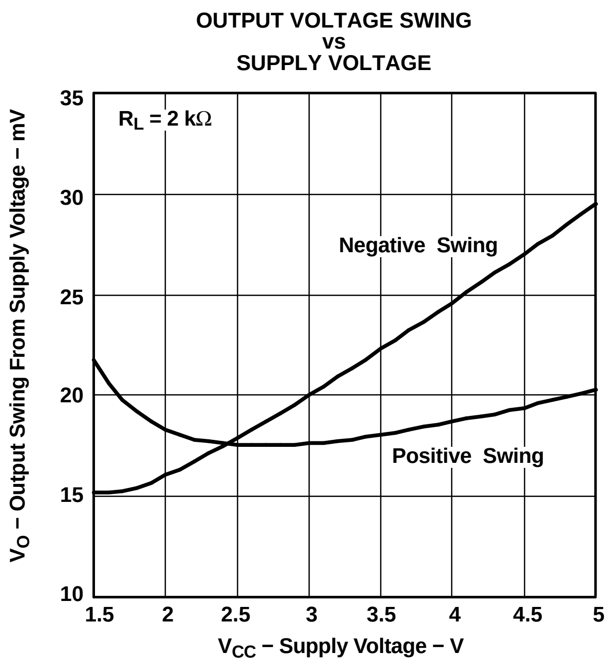


Figure 3.

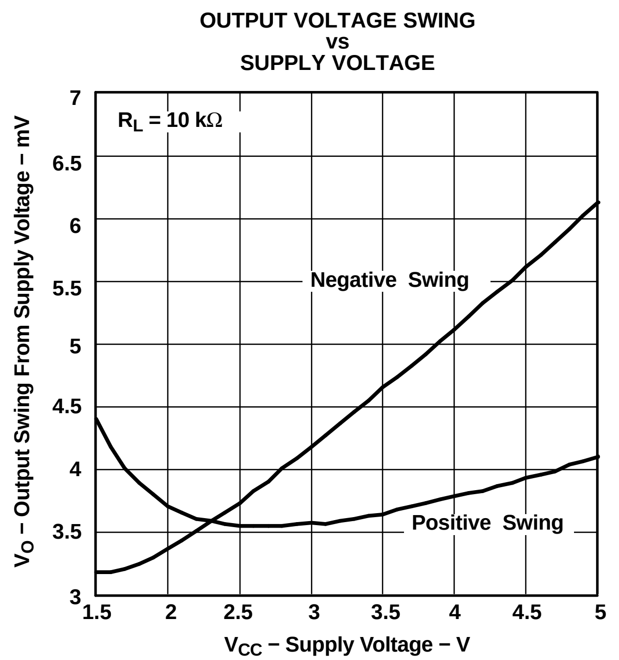


Figure 4.

TYPICAL CHARACTERISTICS (continued)

SOURCE CURRENT
vs
OUTPUT VOLTAGE

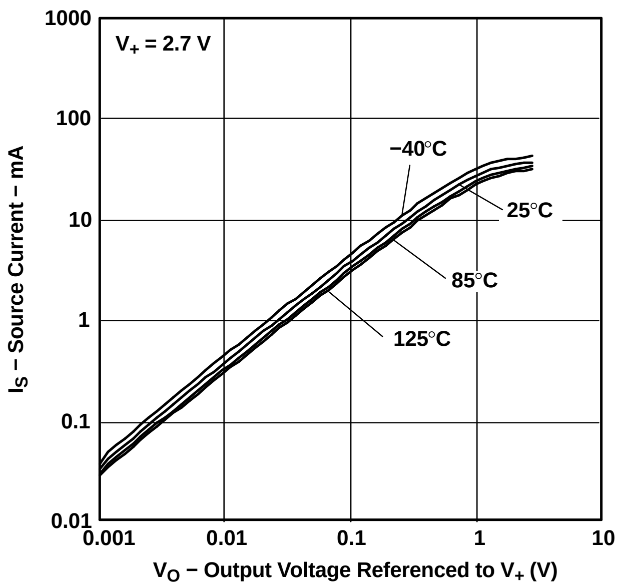


Figure 5.

SOURCE CURRENT
vs
OUTPUT VOLTAGE

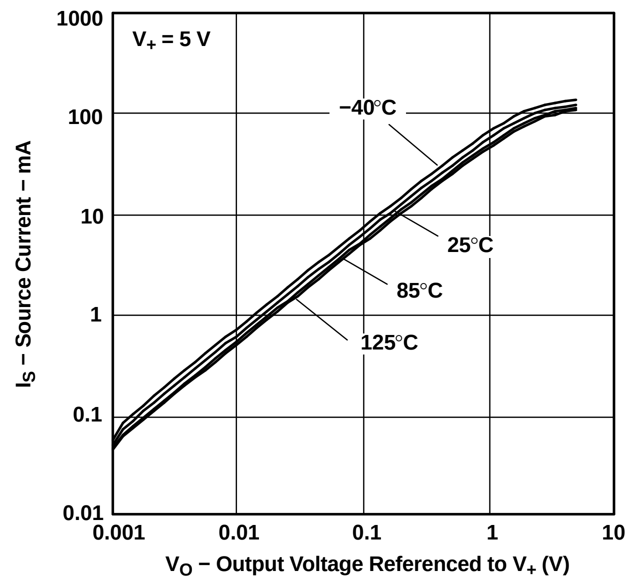


Figure 6.

SINK CURRENT
vs
OUTPUT VOLTAGE

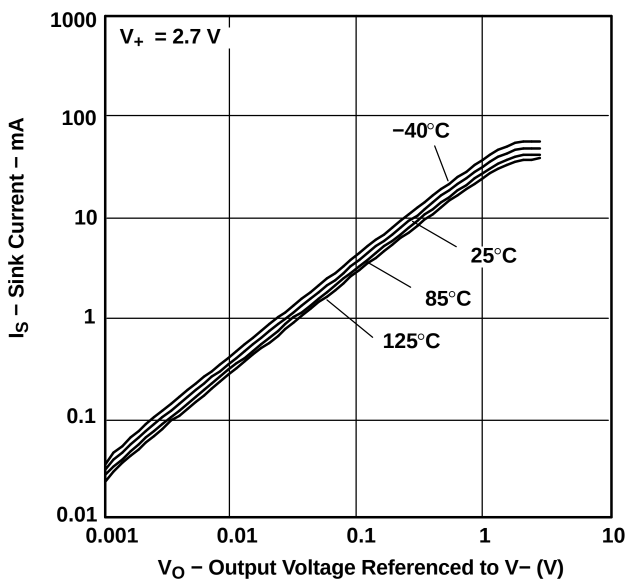


Figure 7.

SINK CURRENT
vs
OUTPUT VOLTAGE

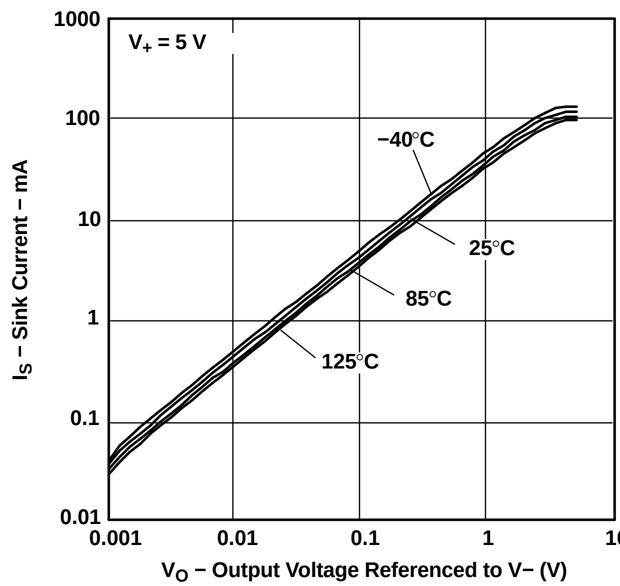


Figure 8.

TYPICAL CHARACTERISTICS (continued)

OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

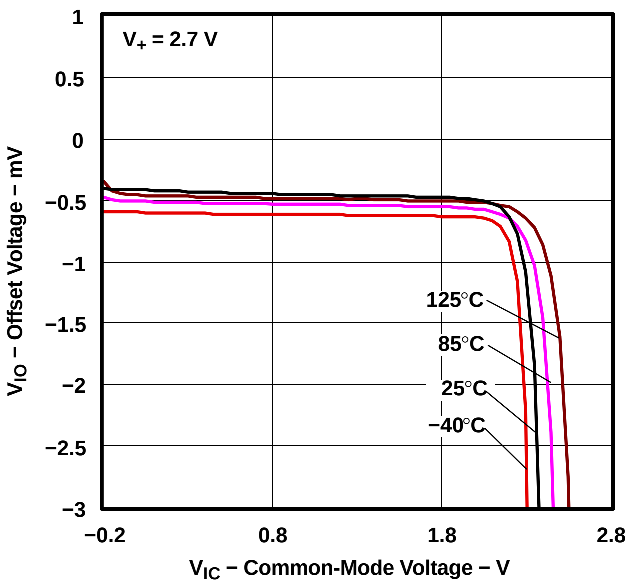


Figure 9.

OFFSET VOLTAGE
vs
COMMON-MODE VOLTAGE

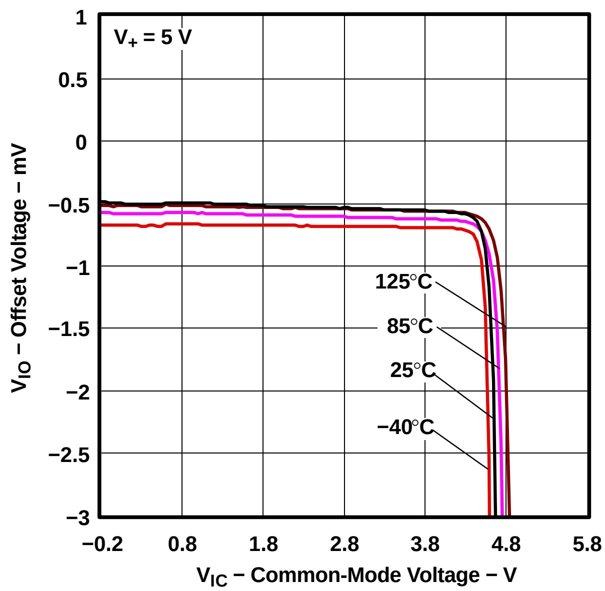


Figure 10.

INPUT VOLTAGE
vs
OUTPUT VOLTAGE

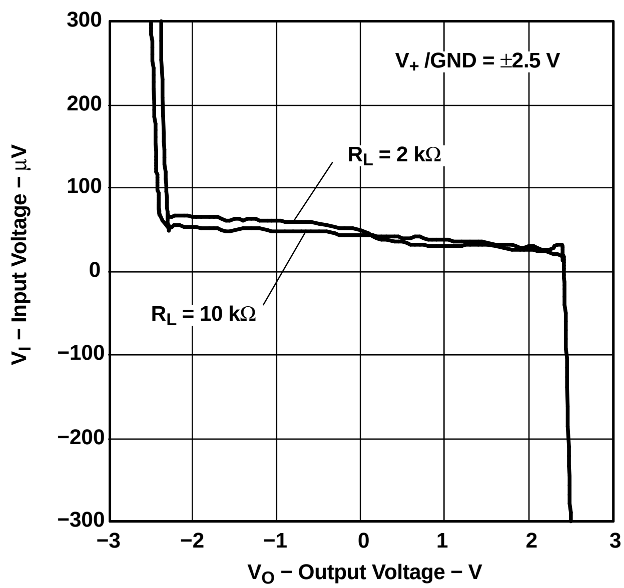


Figure 11.

INPUT VOLTAGE
vs
OUTPUT VOLTAGE

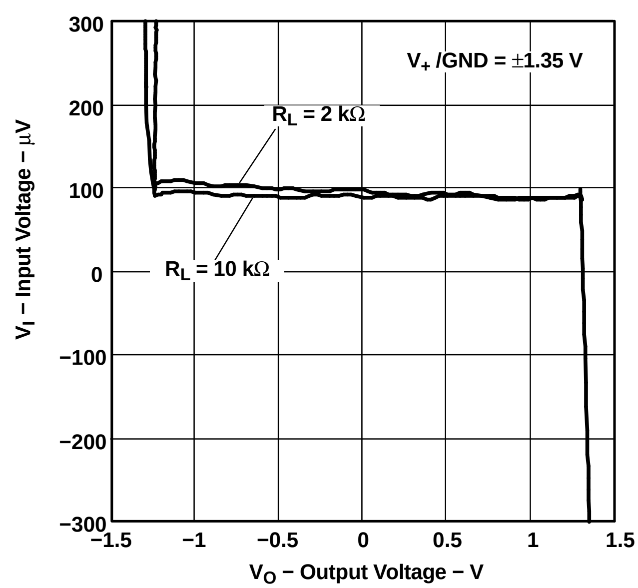


Figure 12.

TYPICAL CHARACTERISTICS (continued)

SLEW RATE
vs
SUPPLY VOLTAGE

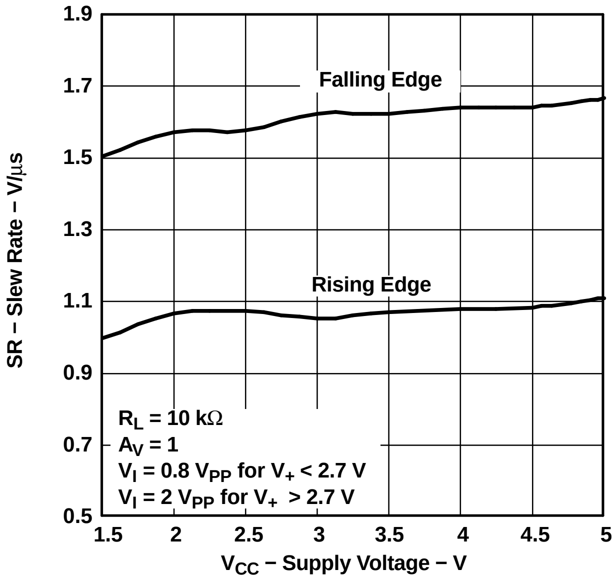


Figure 13.

SLEW RATE
vs
TEMPERATURE

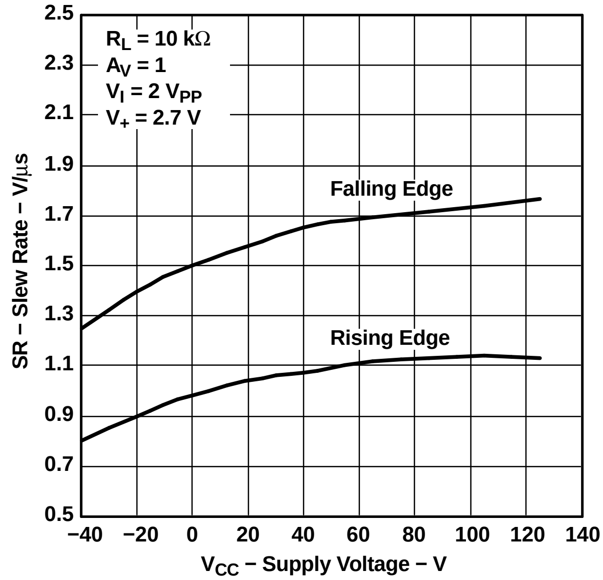


Figure 14.

SLEW RATE
vs
TEMPERATURE

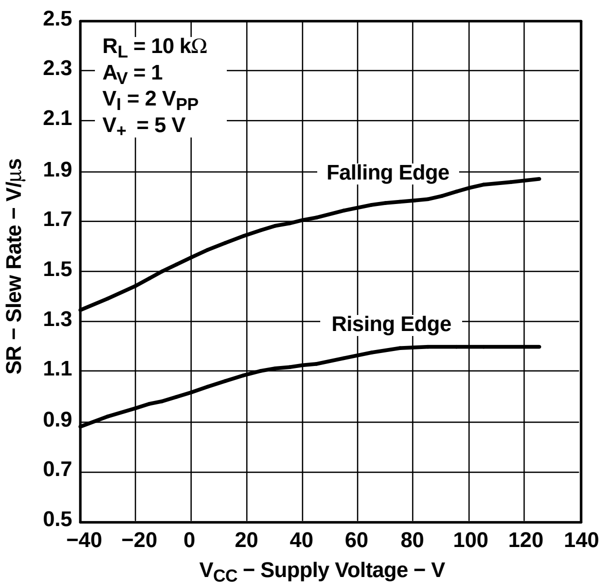


Figure 15.

CMRR
vs
FREQUENCY

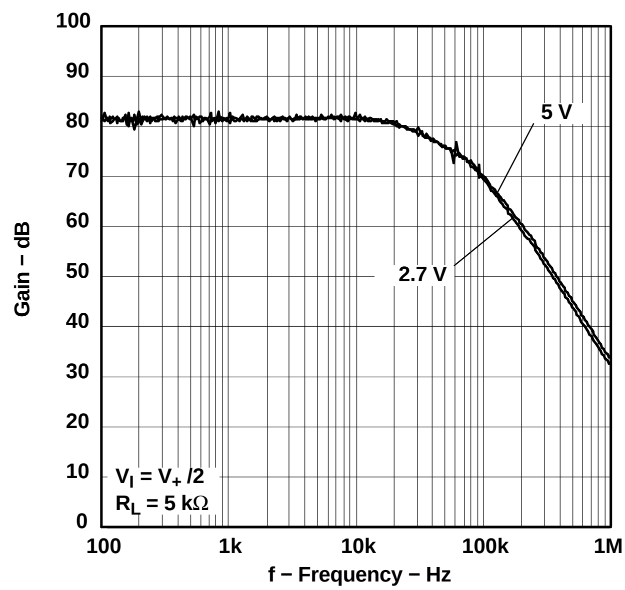


Figure 16.

TYPICAL CHARACTERISTICS (continued)

PSRR
vs
FREQUENCY

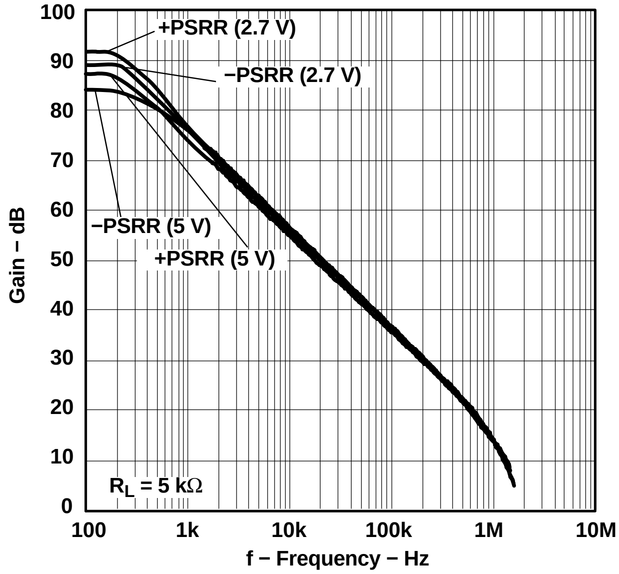


Figure 17.

INPUT VOLTAGE NOISE
vs
FREQUENCY

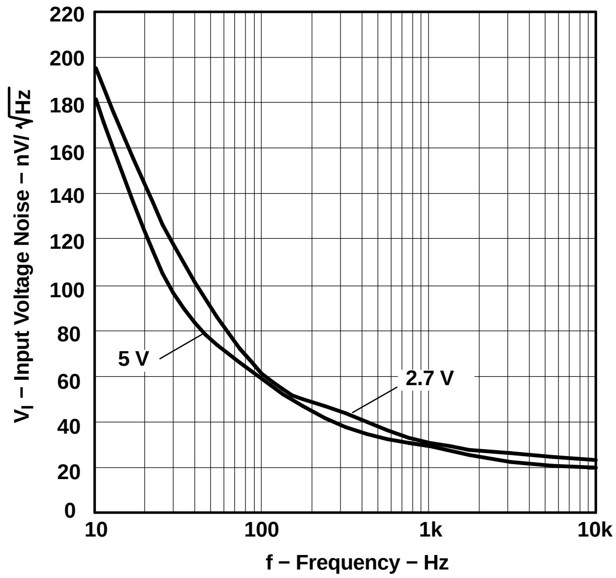


Figure 18.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

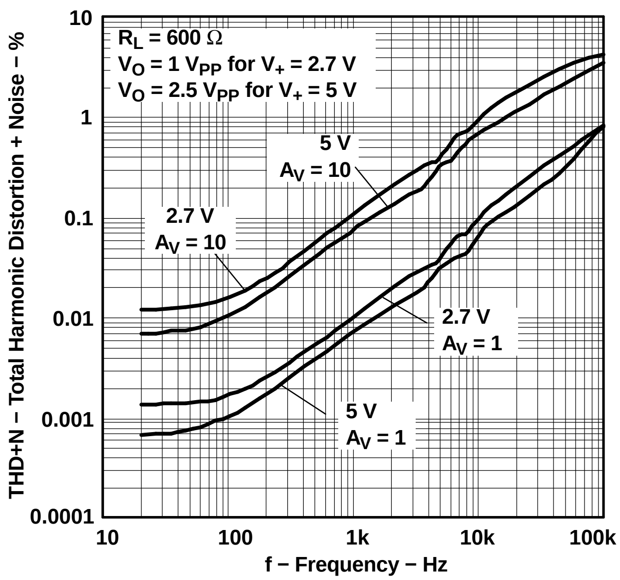


Figure 19.

TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT VOLTAGE

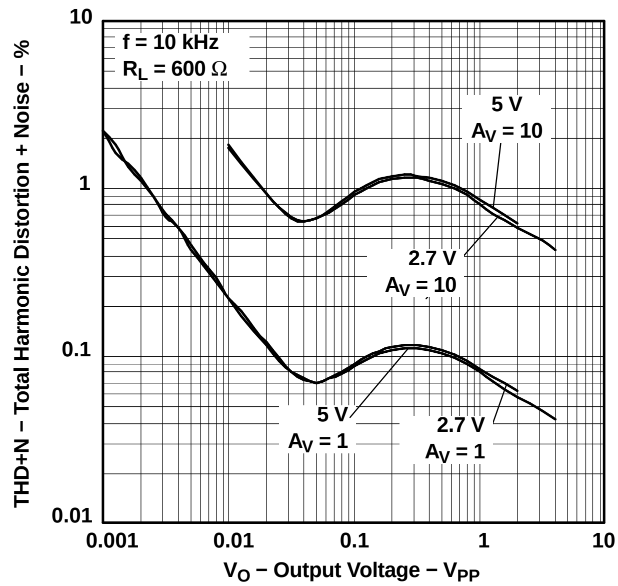


Figure 20.

TYPICAL CHARACTERISTICS (continued)

GAIN AND PHASE MARGIN
vs
FREQUENCY
(T_A = −40°C, 25°C, 125°C)

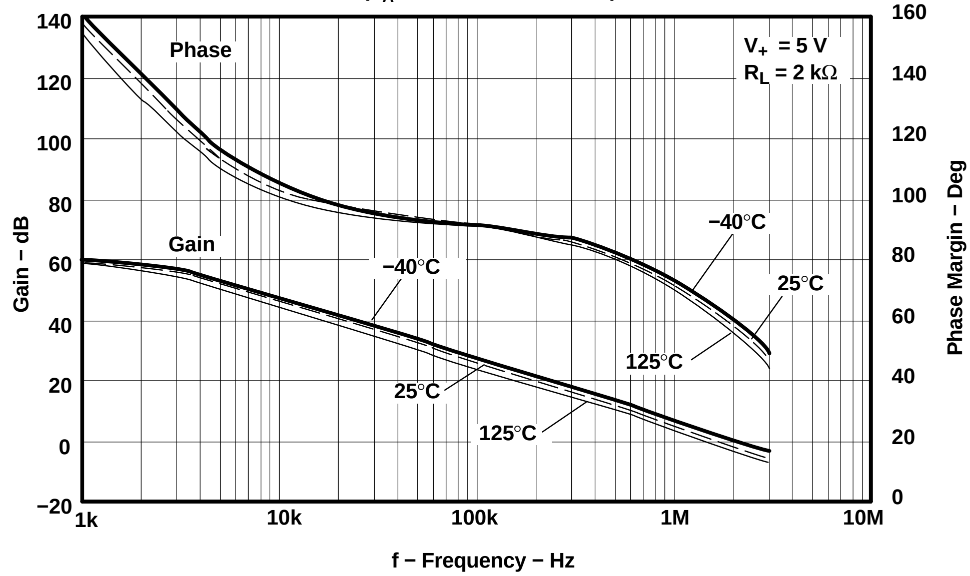


Figure 21.

GAIN AND PHASE MARGIN
vs
FREQUENCY
(R_L = 600 Ω, 2 kΩ, 100 kΩ)

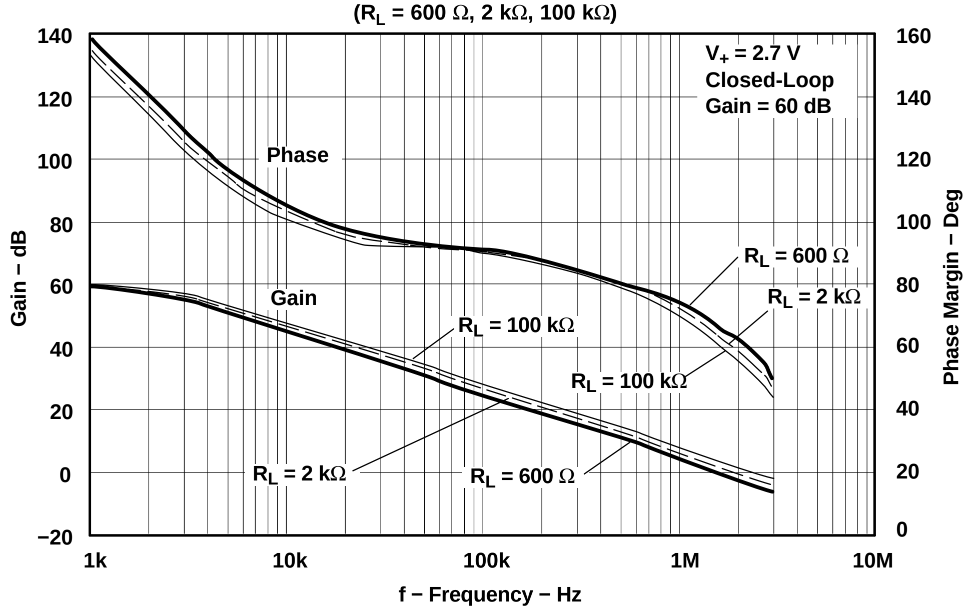


Figure 22.

TYPICAL CHARACTERISTICS (continued)

**GAIN AND PHASE MARGIN
vs
FREQUENCY
(R_L = 600 Ω, 2 kΩ, 100 kΩ)**

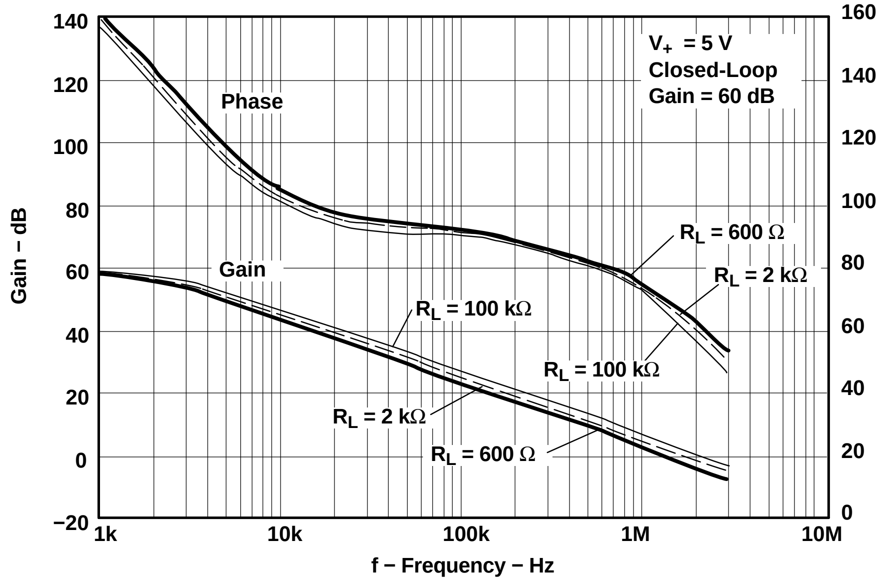


Figure 23.

**GAIN AND PHASE MARGIN
vs
FREQUENCY
(C_L = 0 pF, 100 pF, 500 pF, 1000 pF)**

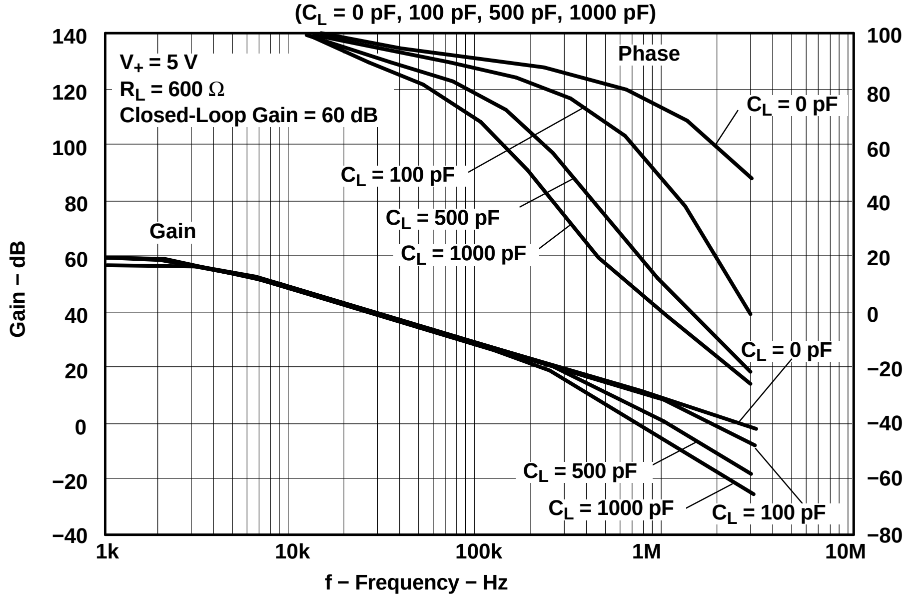


Figure 24.

TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL NONINVERTING RESPONSE

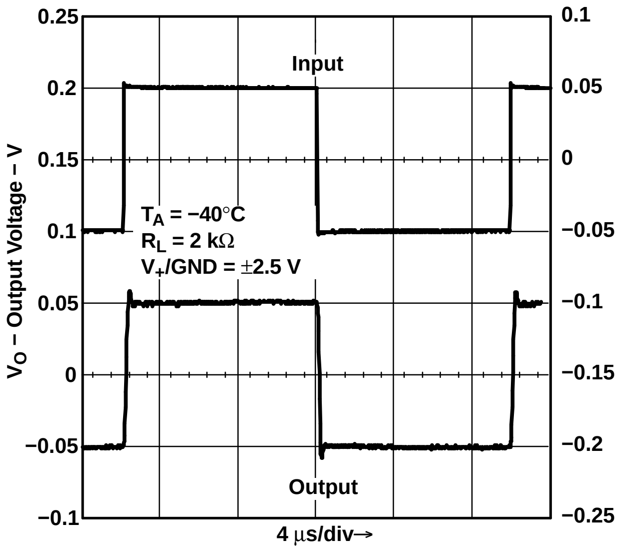


Figure 25.

LARGE-SIGNAL NONINVERTING RESPONSE

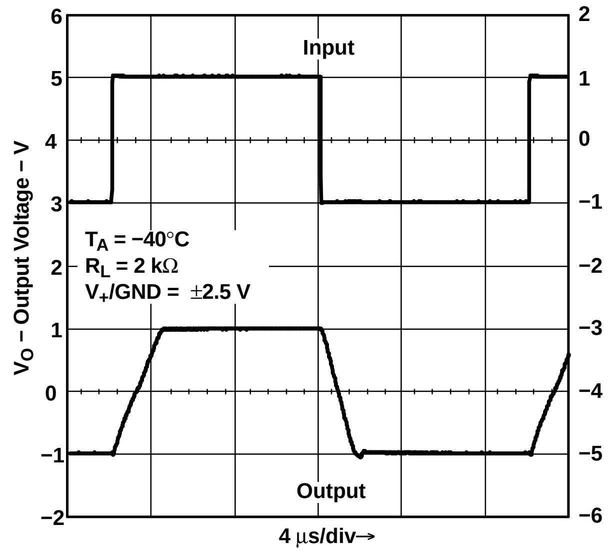


Figure 26.

SMALL-SIGNAL NONINVERTING RESPONSE

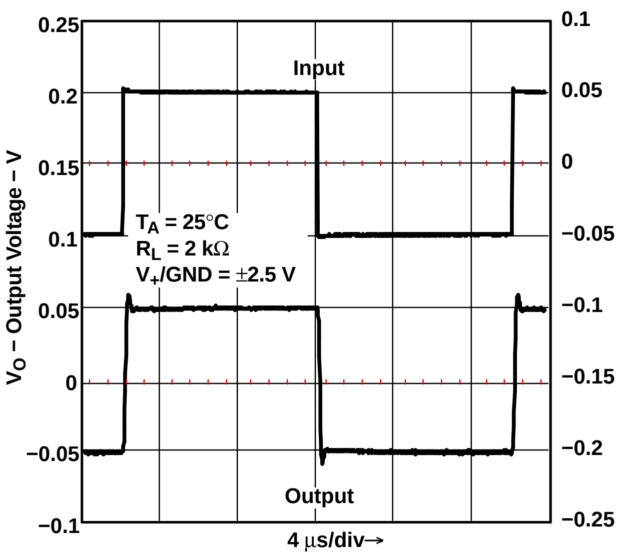


Figure 27.

LARGE-SIGNAL NONINVERTING RESPONSE

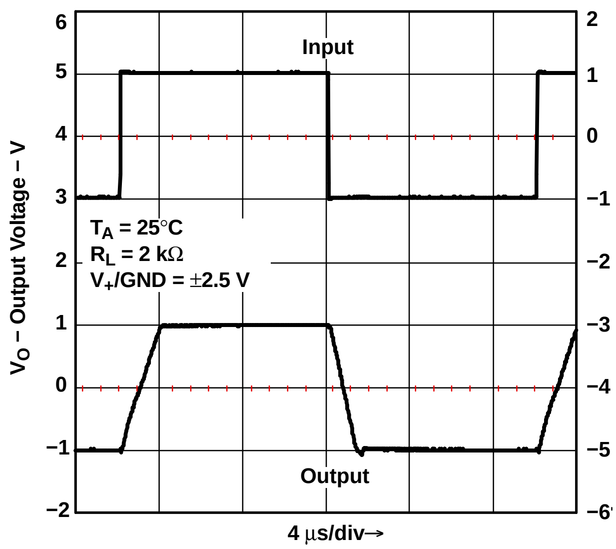


Figure 28.

TYPICAL CHARACTERISTICS (continued)

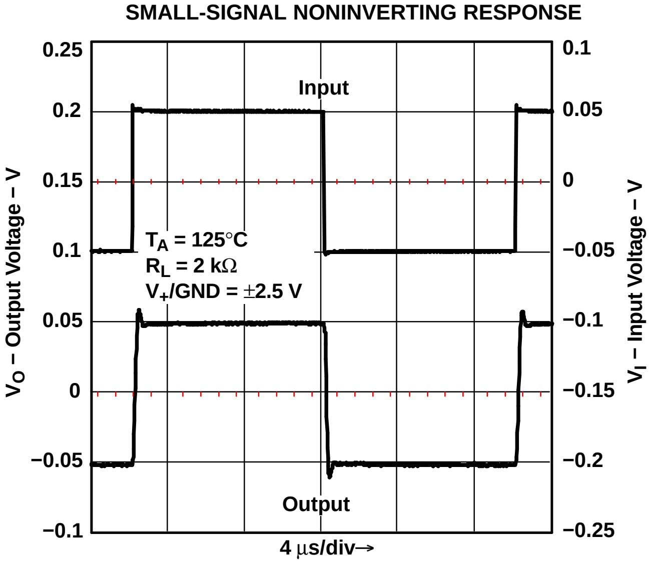


Figure 29.

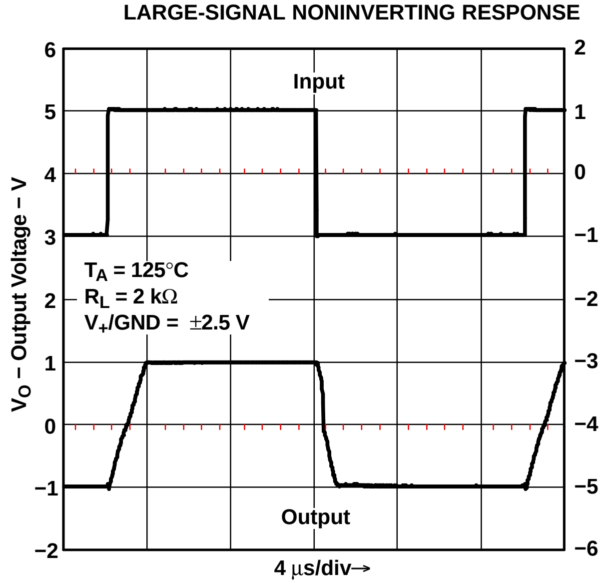


Figure 30.

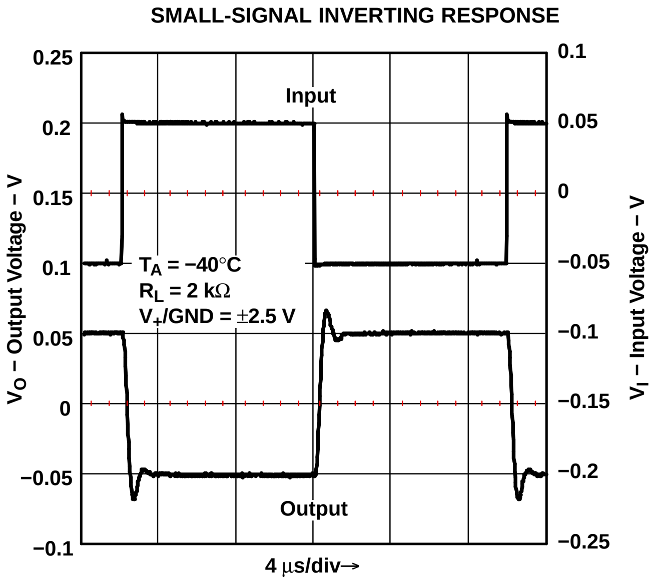


Figure 31.

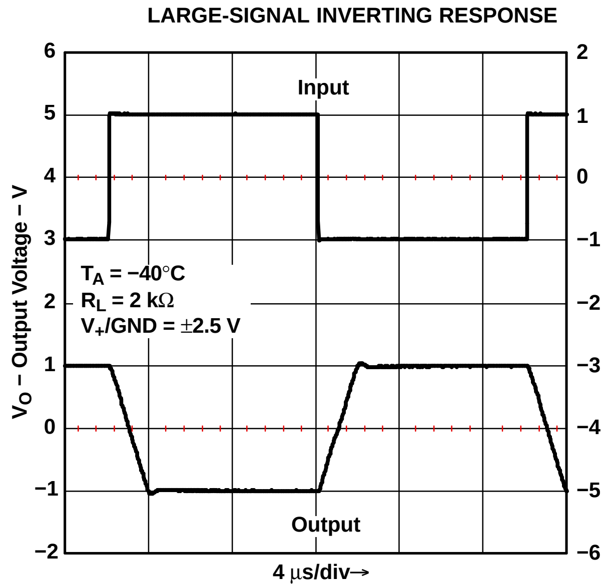


Figure 32.

TYPICAL CHARACTERISTICS (continued)

SMALL-SIGNAL INVERTING RESPONSE

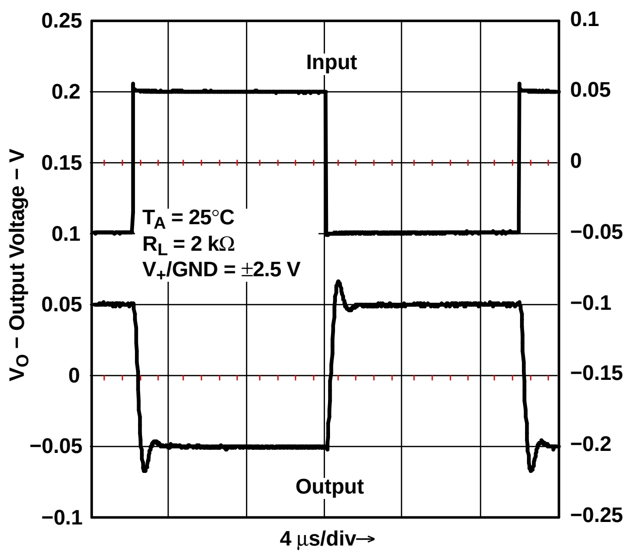


Figure 33.

LARGE-SIGNAL INVERTING RESPONSE

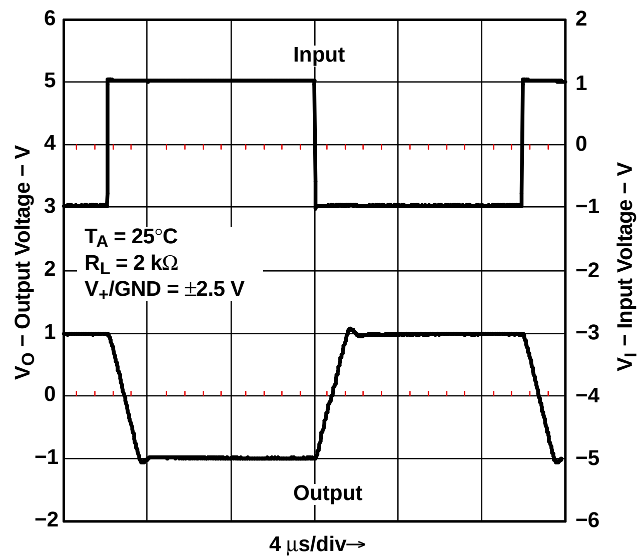


Figure 34.

SMALL-SIGNAL INVERTING RESPONSE

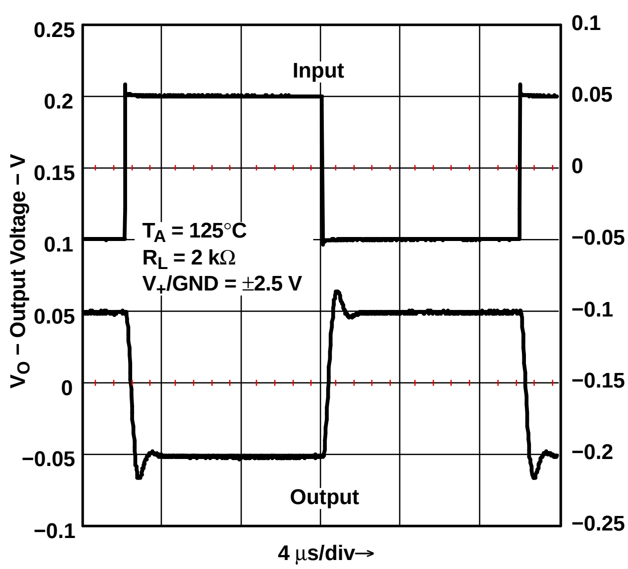


Figure 35.

LARGE-SIGNAL INVERTING RESPONSE

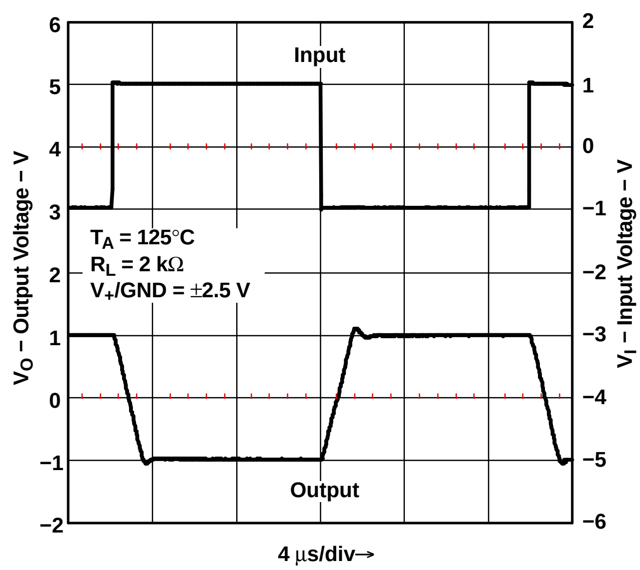


Figure 36.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
LMV341IDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV341IDBVRE4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV341IDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV341IDCKR	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV341IDCKRE4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV341IDCKRG4	ACTIVE	SC70	DCK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV342ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV342IDDUR	PREVIEW	VSSOP	DDU	8	3000	TBD	Call TI	Call TI
LMV342IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV342IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV342IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV342IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV342IDGKT	PREVIEW	MSOP	DGK	8	250	TBD	Call TI	Call TI
LMV342IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV342IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV342IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
						no Sb/Br)		
LMV344IPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LMV344IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMV344 :

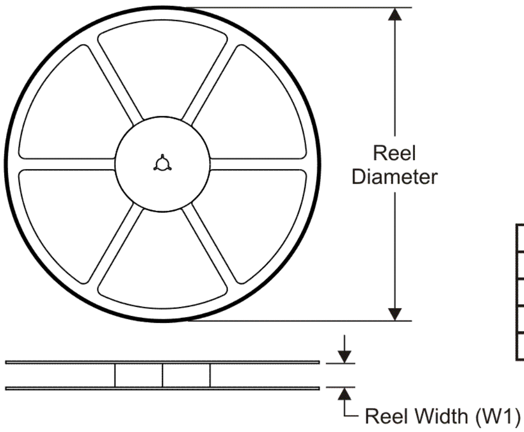
- Automotive: LMV344-Q1

NOTE: Qualified Version Definitions:

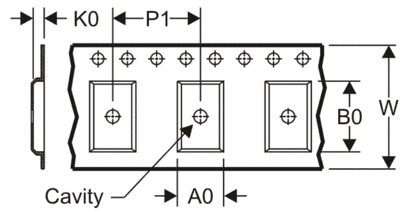
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

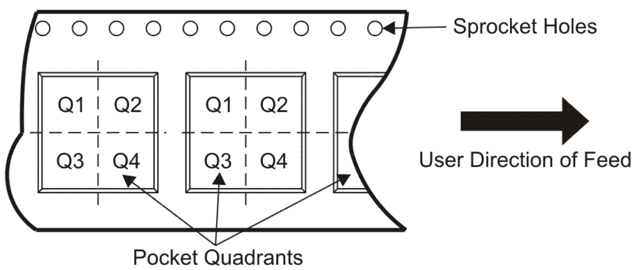


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

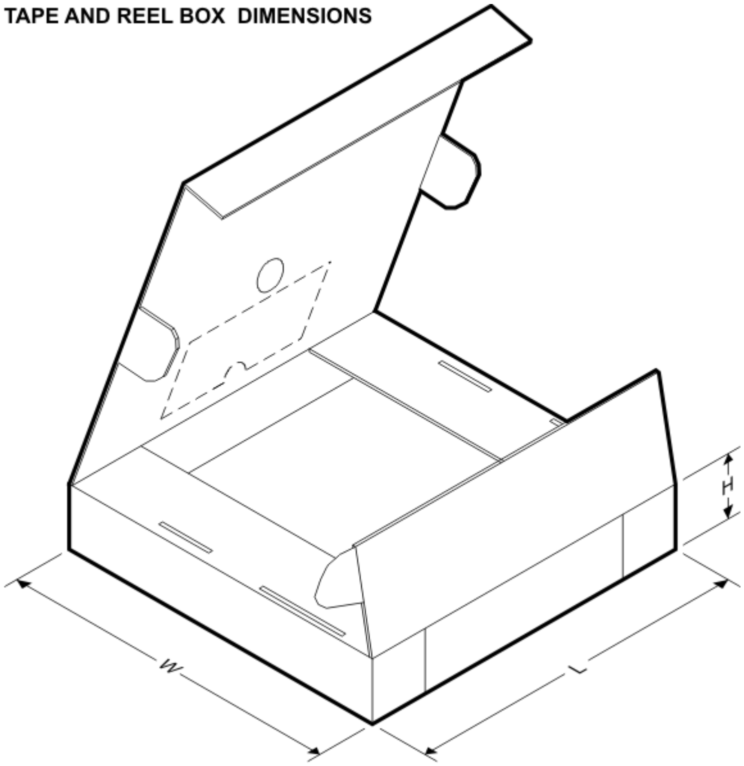
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV341IDBVR	SOT-23	DBV	6	3000	180.0	9.2	3.23	3.17	1.37	4.0	8.0	Q3
LMV341IDBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV341IDCKR	SC70	DCK	6	3000	180.0	8.4	2.24	2.34	1.22	4.0	8.0	Q3
LMV342IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMV342IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LMV344IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LMV344IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

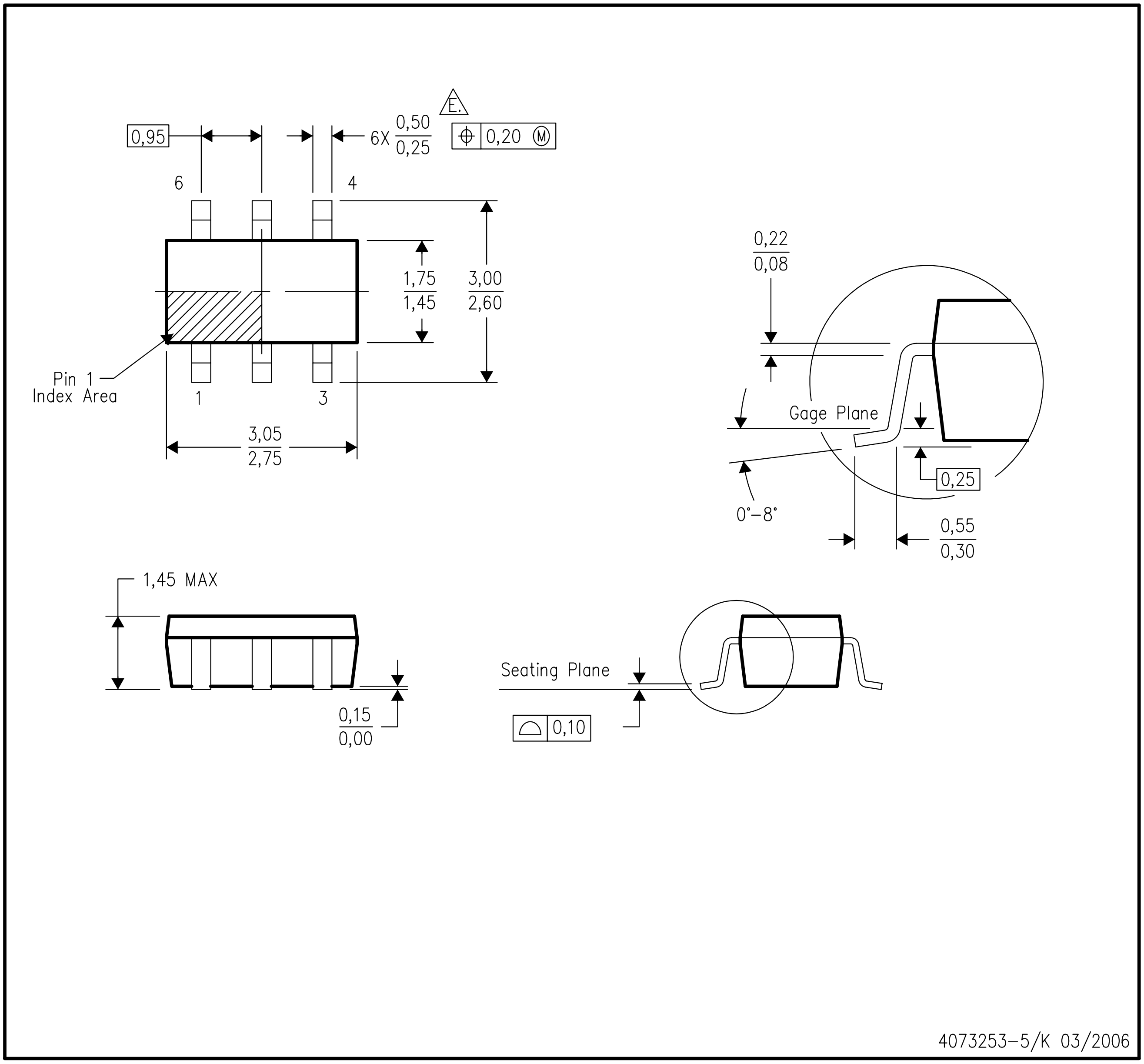
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

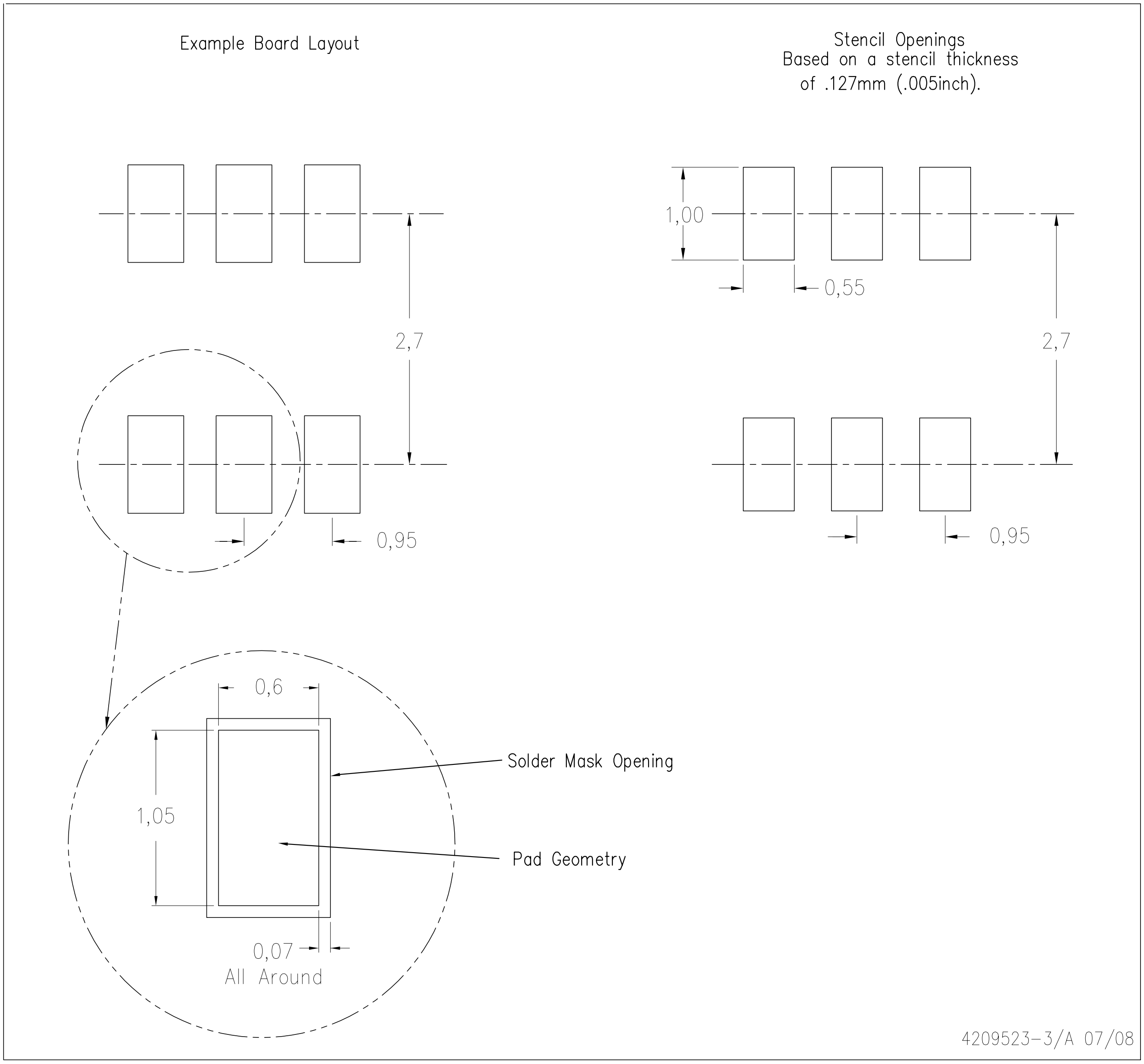
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV341IDBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
LMV341IDBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
LMV341IDCKR	SC70	DCK	6	3000	202.0	201.0	28.0
LMV342IDGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
LMV342IDR	SOIC	D	8	2500	340.5	338.1	20.6
LMV344IDR	SOIC	D	14	2500	346.0	346.0	33.0
LMV344IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



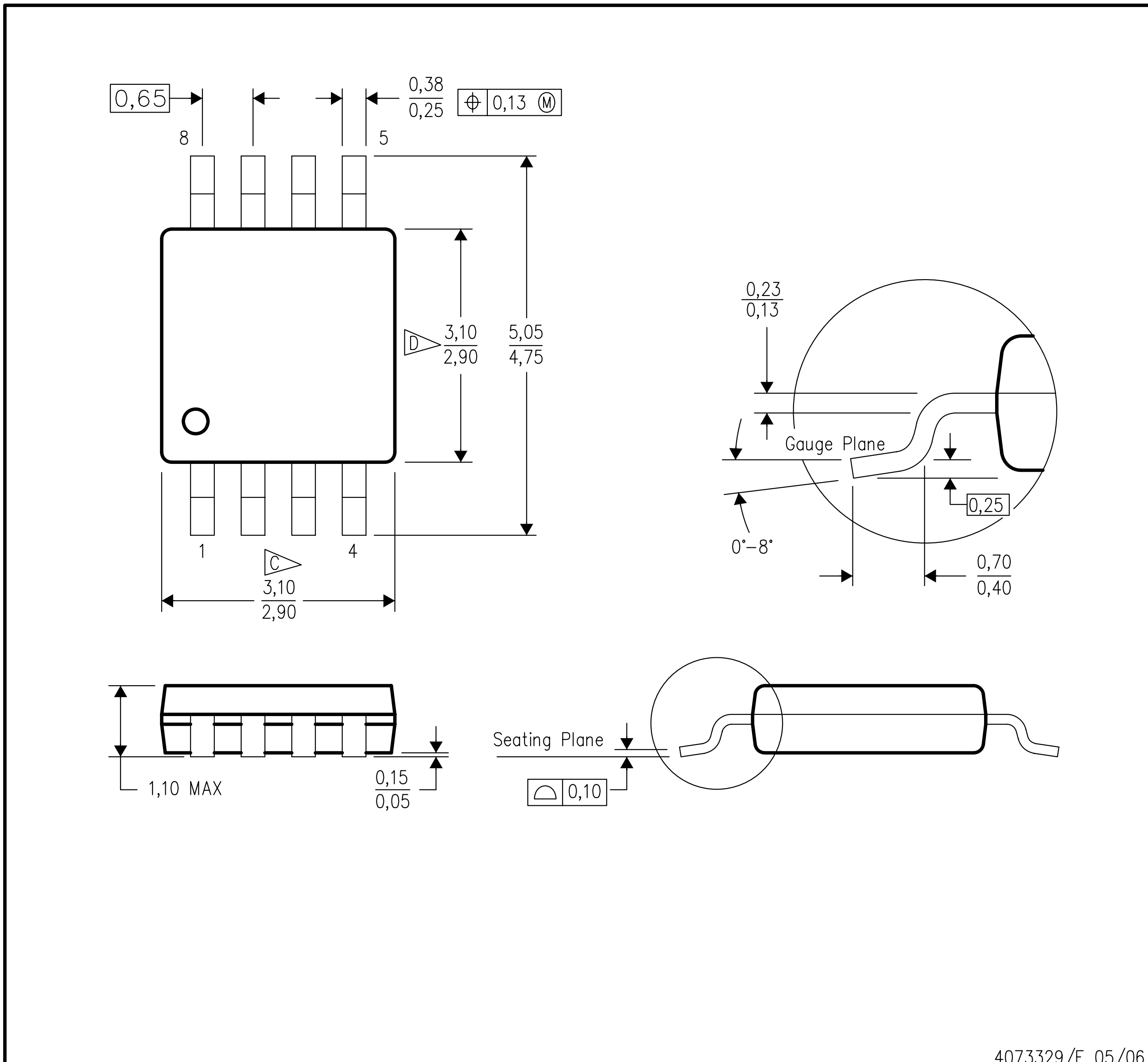
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)



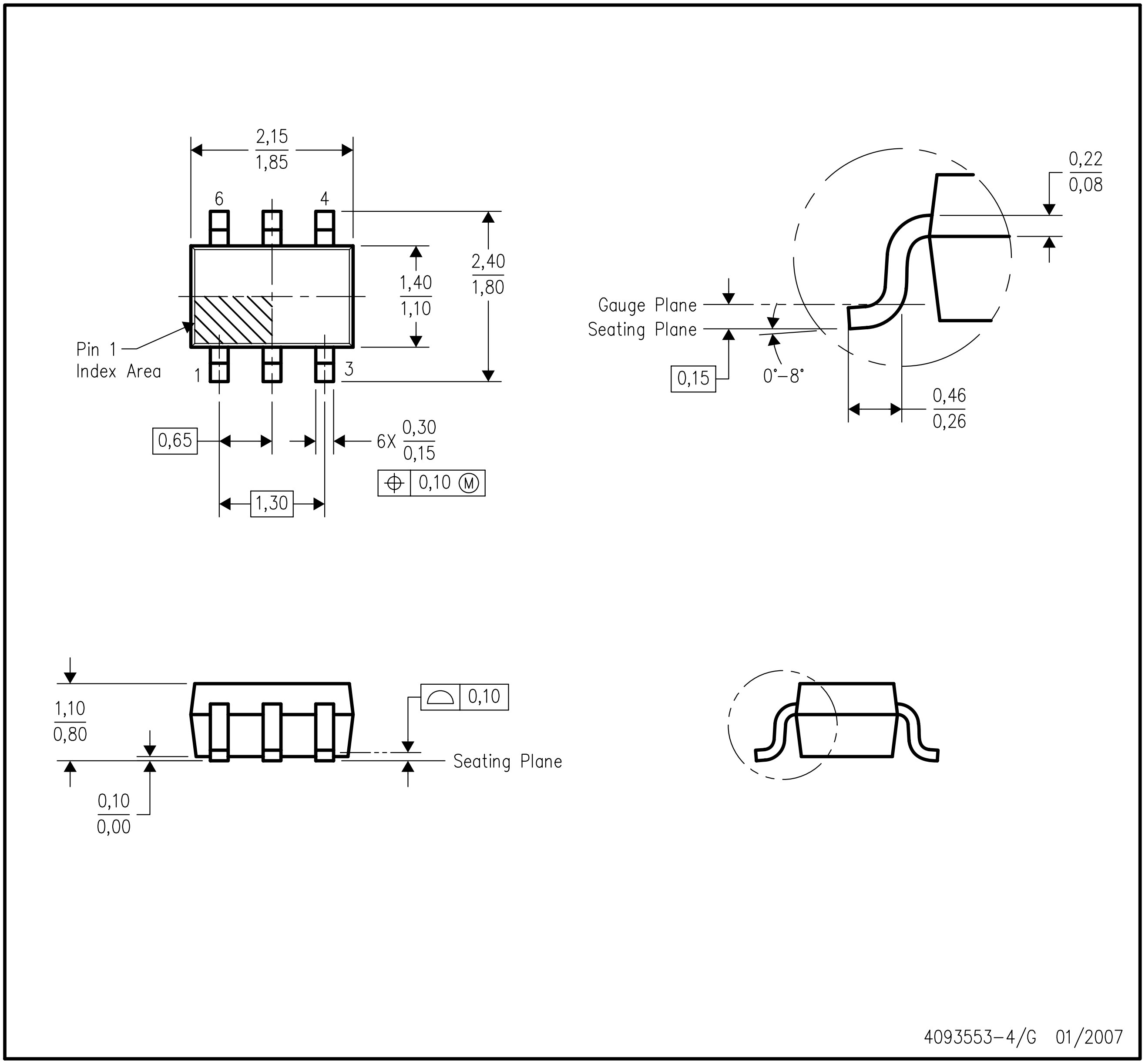
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



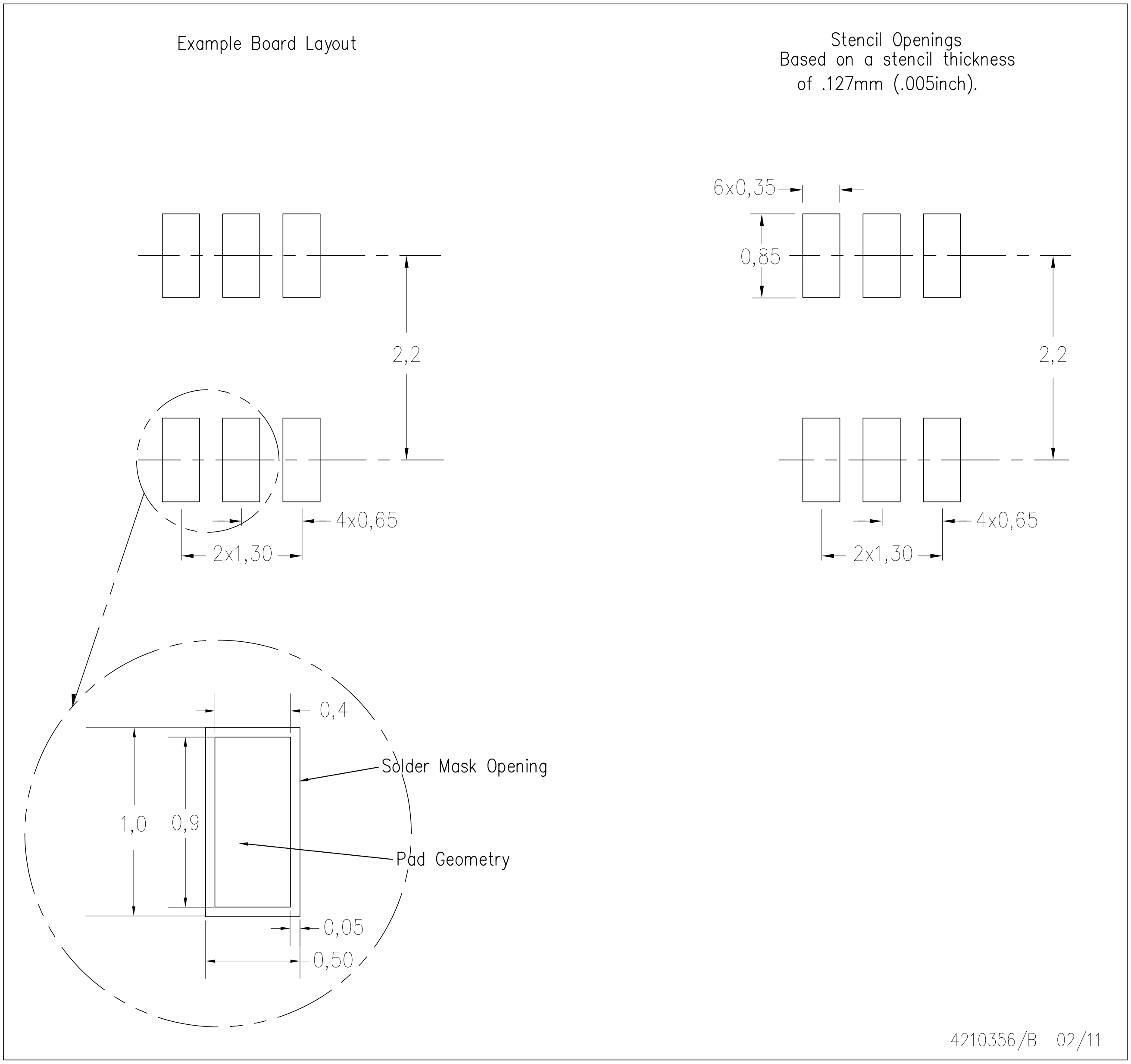
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DCK (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



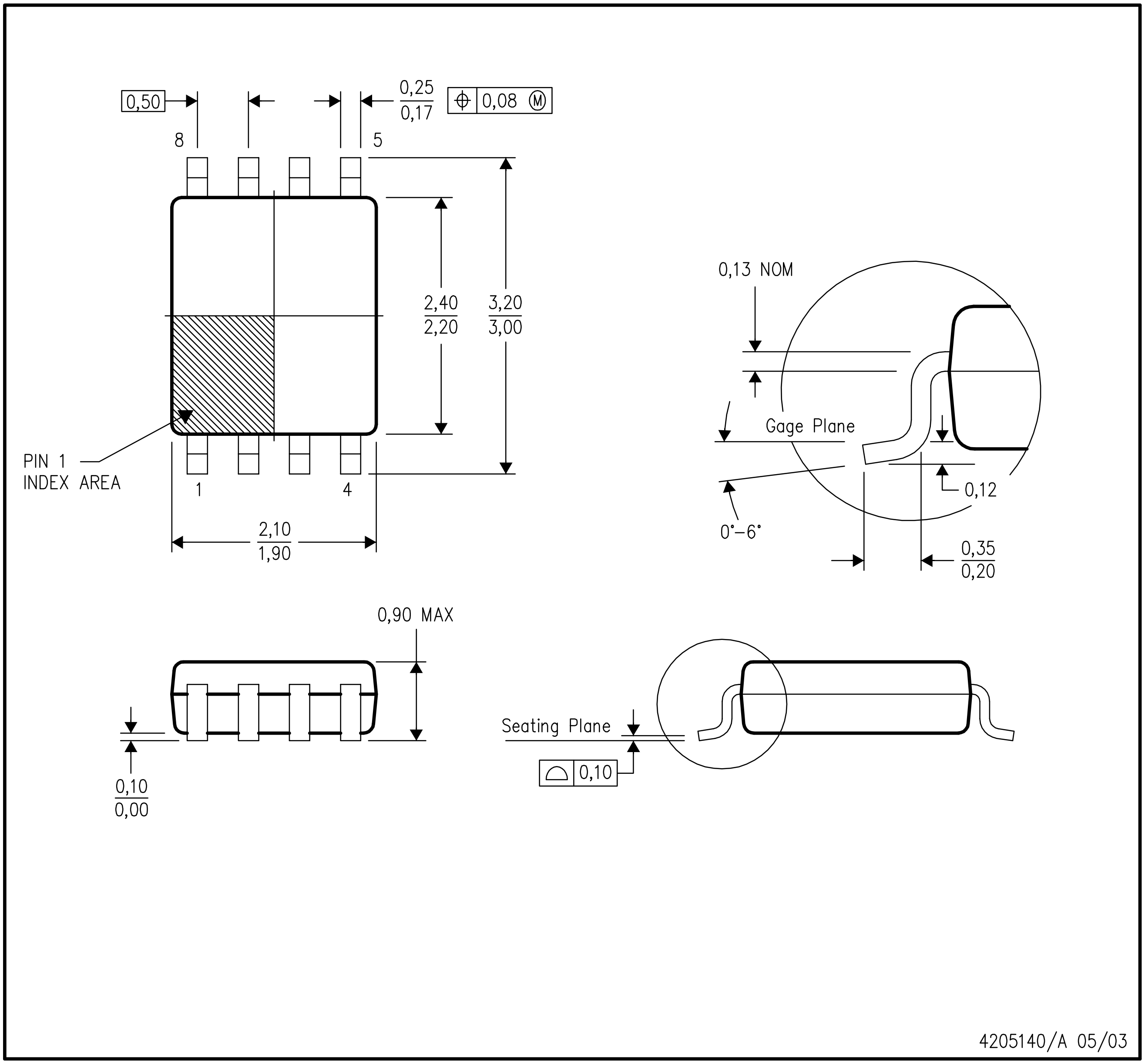
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6) PLASTIC SMALL OUTLINE



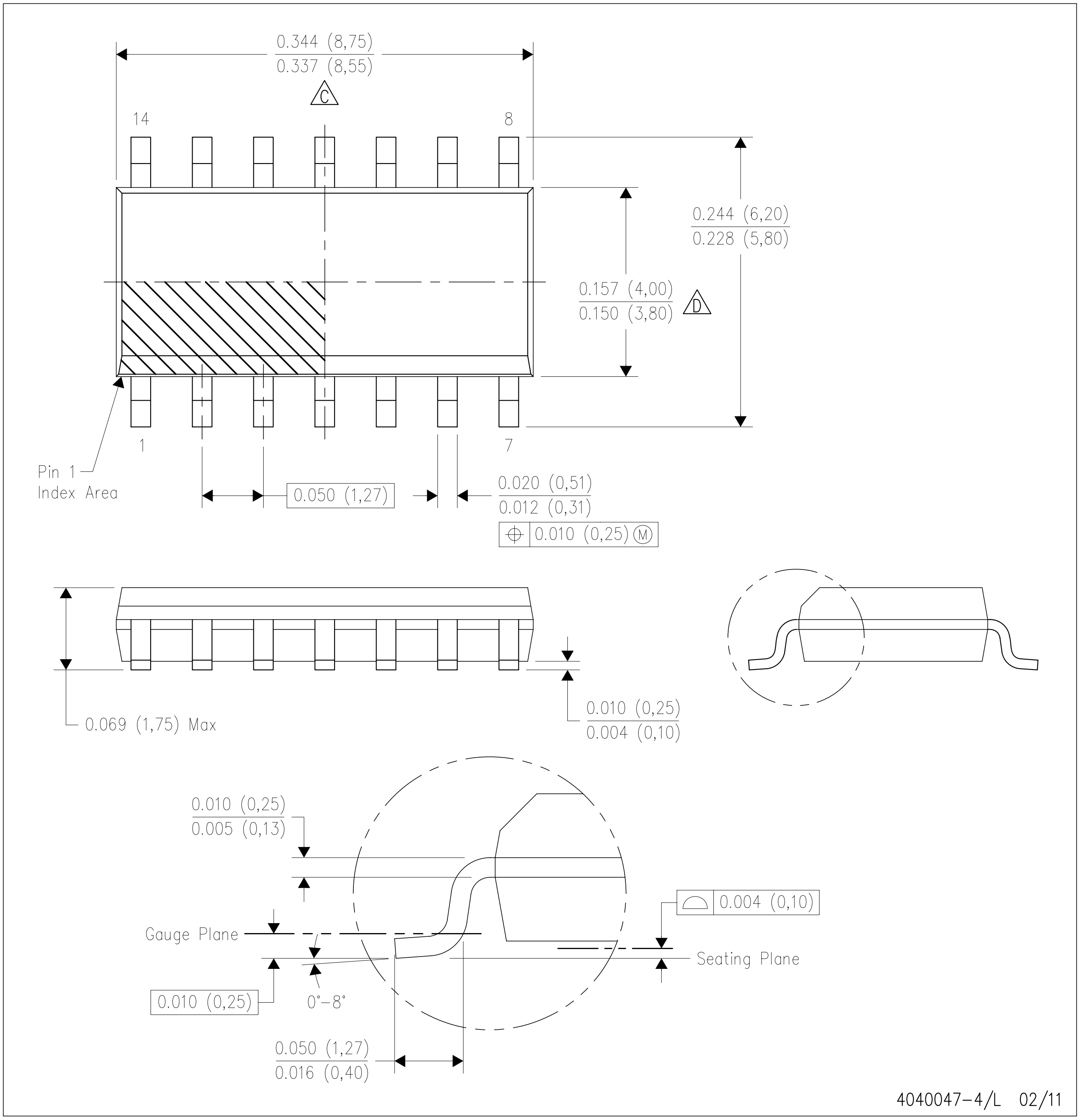
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DDU (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



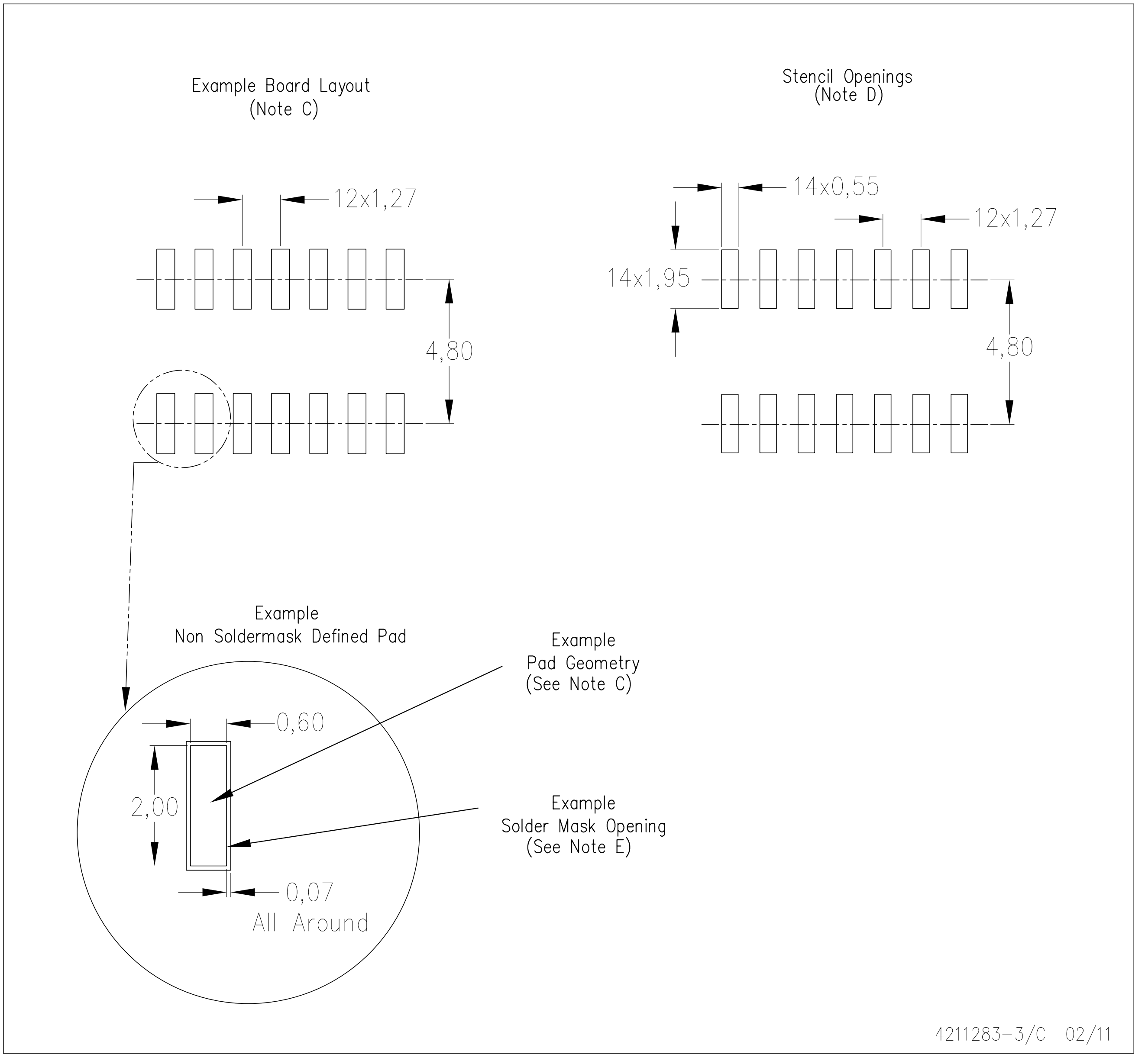
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-187 variation CA.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



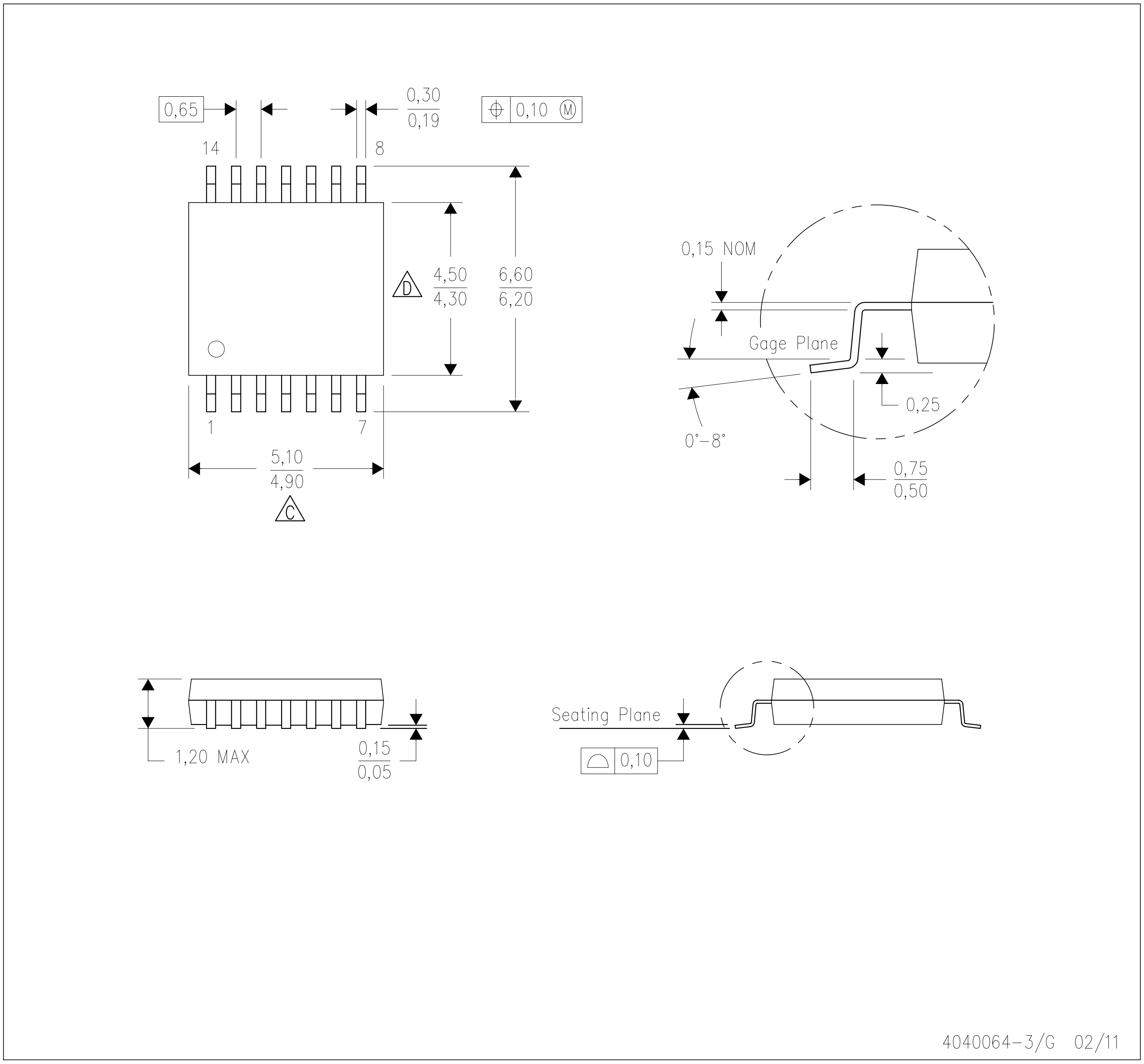
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



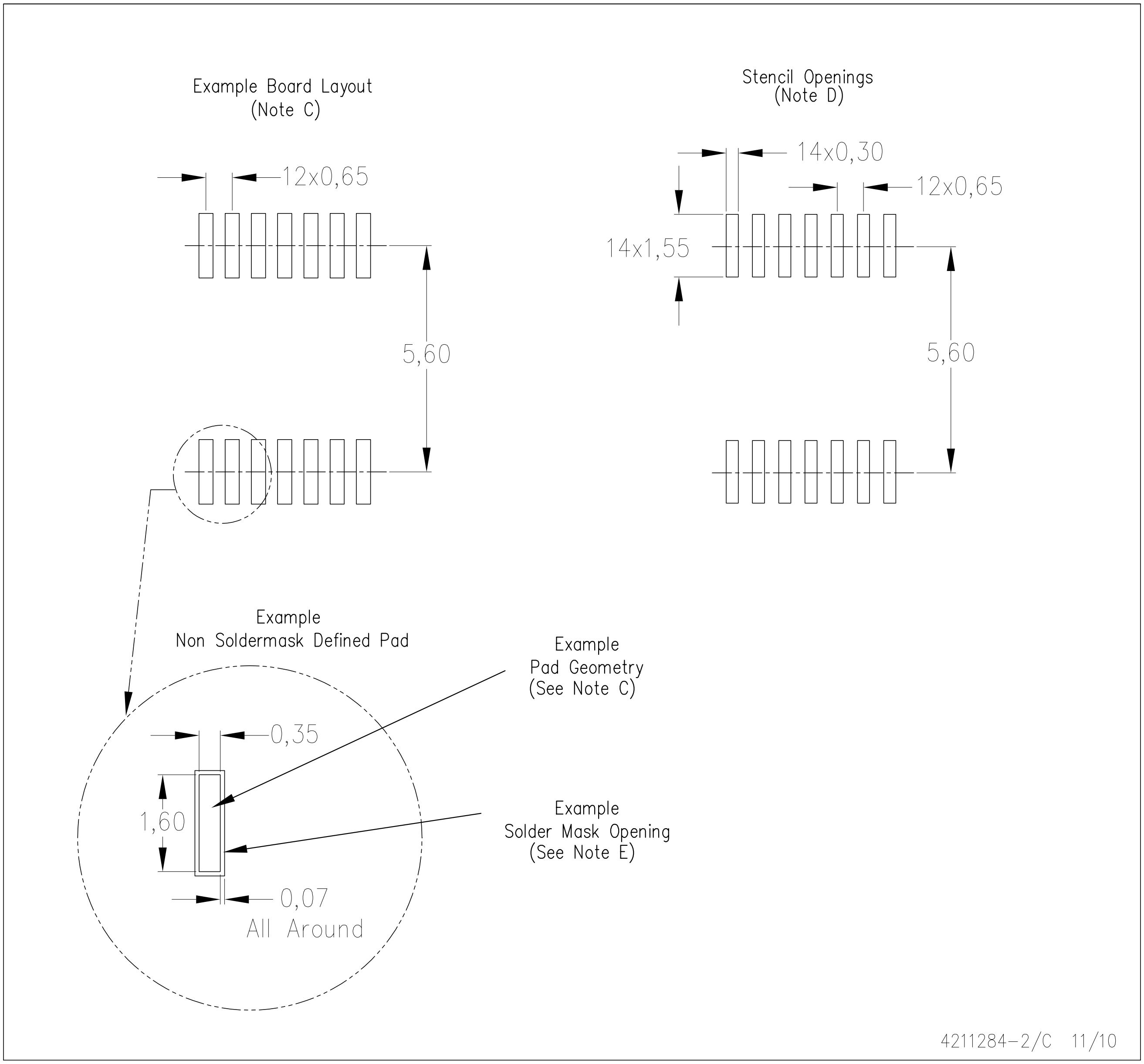
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



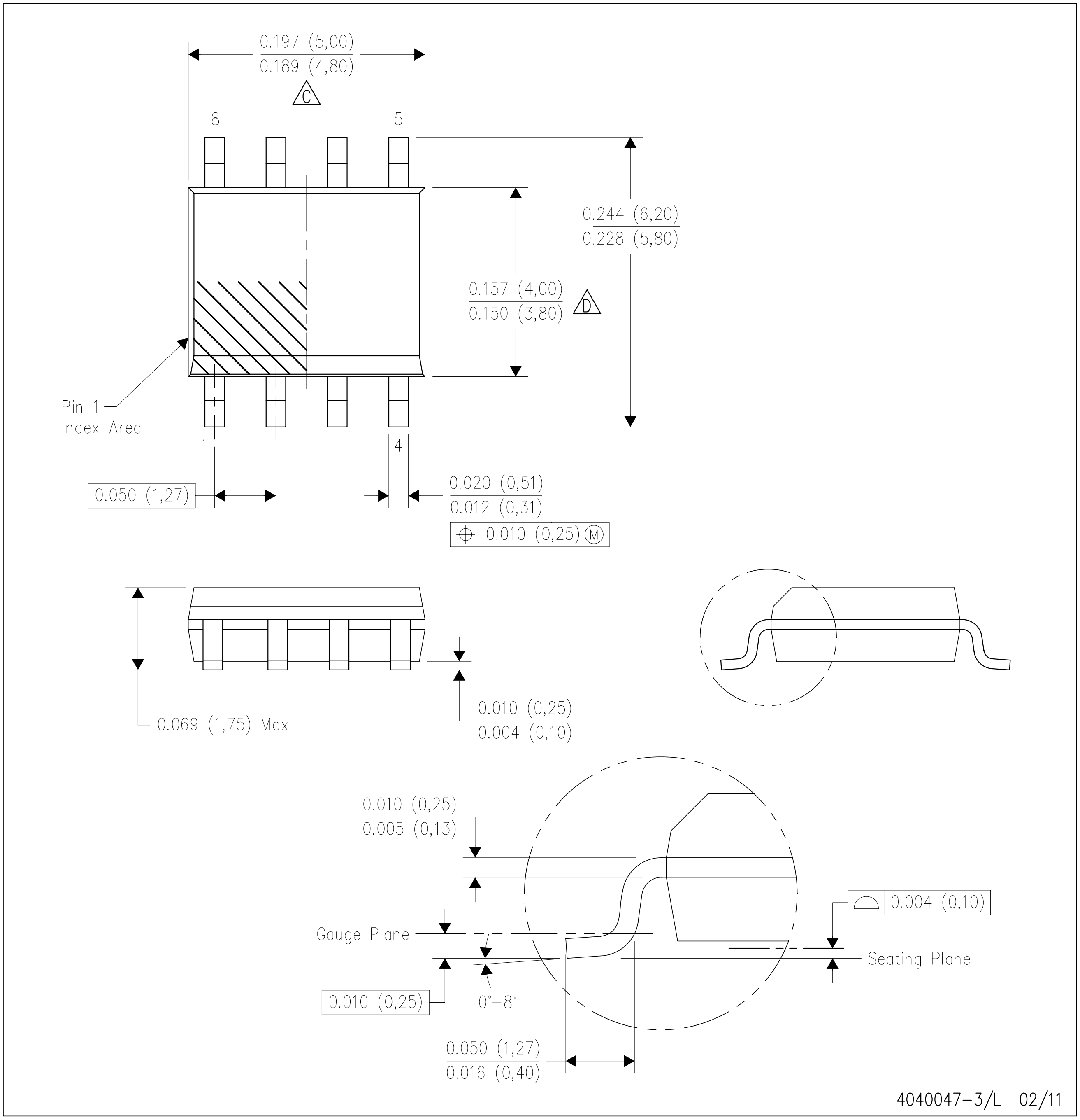
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



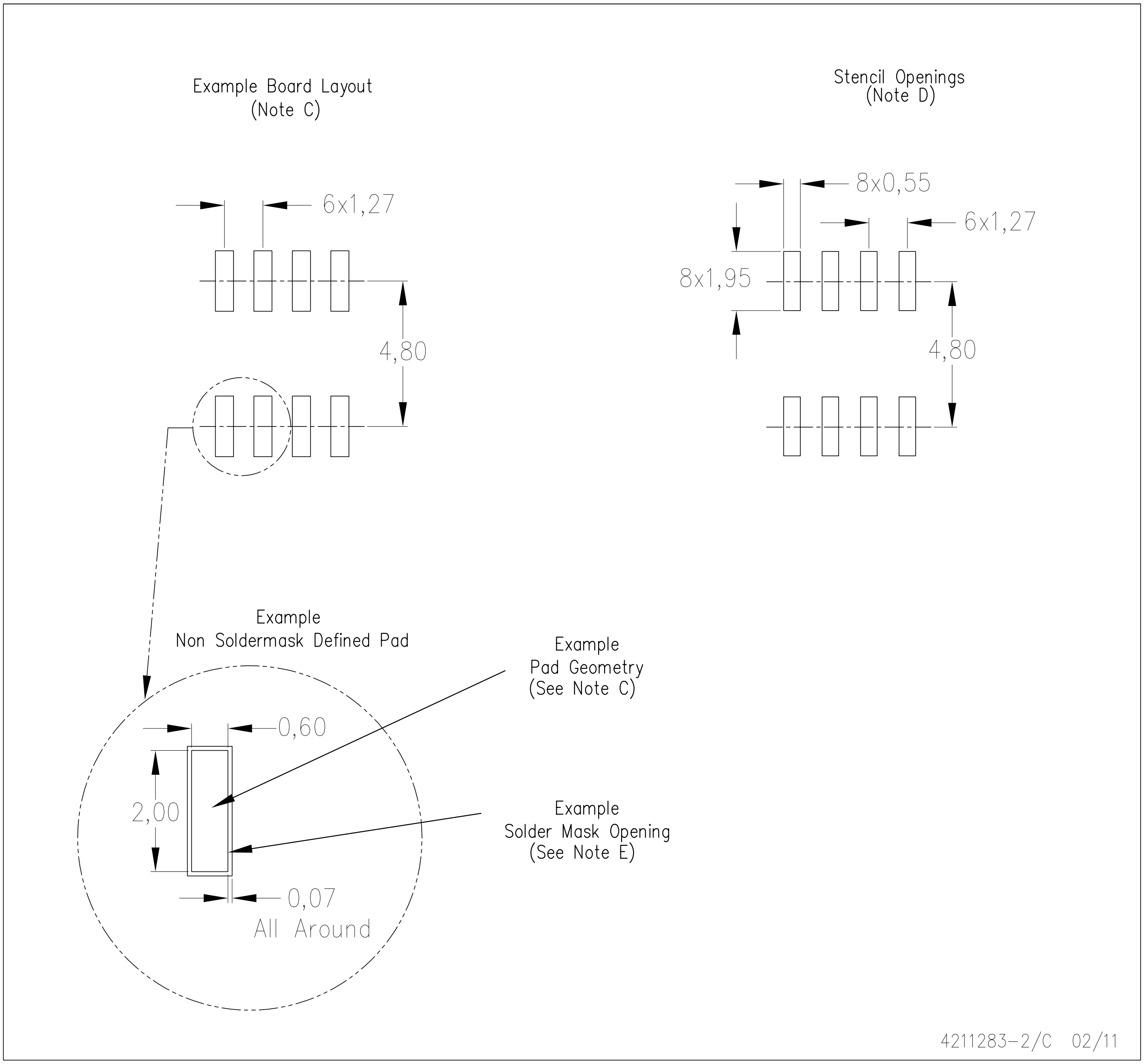
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.