Value Line Transceiver

Applications

- Ultra low-power wireless applications operating in the 315/433/868/915 MHz ISM/SRD bands
- Wireless alarm and security systems
- Industrial monitoring and control
- Remote Controls
- Toys
- Home and building automation

Key Features

RF Performance

- Programmable output power up to +12dBm
- Receive sensitivity down to −116 dBm at 0.6 kbps
- Programmable data rate from 0.6 to 600 kbps
- Frequency bands: 300 - 348 MHz, 387 - 464 MHz, and 779 - 928 MHz
- 2-FSK, 4-FSK, GFSK, and OOK supported

Digital Features

- Flexible support for packet oriented systems
- On-chip support for sync word detection, flexible packet length, and automatic CRC calculation

Low-Power Features

- 200 nA sleep mode current consumption
- Fast start-up time; 240 µs from sleep to RX or TX mode
- 64-byte RX and TX FIFO

Improved Range using CC1190

- The ***CC1190*** [13] is a range extender for 850 - 950 MHz and is an ideal fit for ***CC110L*** to enhance RF performance
- High sensitivity
  - –118 dBm at 1.2 kBaud, 868 MHz, 1% packet error rate
  - –120 dBm at 1.2 kBaud, 915 MHz, 1% packet error rate
- +20 dBm output power at 868 MHz
- +26 dBm output power at 915 MHz

General

- Few external components; Completely on-chip frequency synthesizer, no external filters or RF switch needed
- Green package: RoHS compliant and no antimony or bromine
- Small size (QLP 4x4 mm package, 20 pins)
- Suited for systems targeting compliance with EN 300 220 V2.3.1 (Europe) and FCC CFR Part 15 (US)
- Support for asynchronous and synchronous serial transmit mode for backwards compatibility with existing radio communication protocols

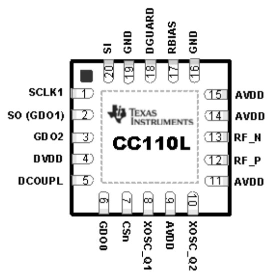
Product Description

The ***CC110L*** is a cost optimized sub-1 GHz RF transceiver for the 300 - 348 MHz, 387 - 464 MHz, and 779 - 928 MHz frequency bands. The circuit is based on the popular ***CC1101*** RF transceiver, and RF performance characteristics are identical. Two ***CC110L*** transceivers together enable a low cost bidirectional RF link.

The RF transceiver is integrated with a highly configurable baseband modem. The modem supports various modulation formats and has a configurable data rate up to 600 kbps.

CC110L provides extensive hardware support for packet handling, data buffering and burst transmissions.

The main operating parameters and the 64-byte receive and transmit FIFOs of ***CC110L*** can be controlled via an SPI interface. In a typical system, the ***CC110L*** will be used together with a microcontroller and a few additional passive components.



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implantable cardiac rhythm management systems, including without limitation pacemakers, defibrillators and cardiac resynchronization devices,
external cardiac rhythm management systems that communicate directly with one or more implantable medical devices; or
other devices used to monitor or treat cardiac function, including without limitation pressure sensors, biochemical sensors and neurostimulators.
Please contact lpw-medical-approval@list.ti.com if your application might fall within the category described above.

Abbreviations

Abbreviations used in this data sheet are described below.

2-FSK	Binary Frequency Shift Keying
ADC	Analog to Digital Converter
AFC	Automatic Frequency Compensation
AGC	Automatic Gain Control
AMR	Automatic Meter Reading
BER	Bit Error Rate
BT	Bandwidth-Time product
CCA	Clear Channel Assessment
CFR	Code of Federal Regulations
CRC	Cyclic Redundancy Check
CS	Carrier Sense
CW	Continuous Wave (Unmodulated Carrier)
DC	Direct Current
DVGA	Digital Variable Gain Amplifier
ESR	Equivalent Series Resistance
FCC	Federal Communications Commission
FHSS	Frequency Hopping Spread Spectrum
FS	Frequency Synthesizer
GFSK	Gaussian shaped Frequency Shift Keying
IF	Intermediate Frequency
I/Q	In-Phase/Quadrature
ISM	Industrial, Scientific, Medical
LC	Inductor-Capacitor
LNA	Low Noise Amplifier
LO	Local Oscillator
LSB	Least Significant Bit
MCU	Microcontroller Unit
MSB	Most Significant Bit
NRZ	Non Return to Zero (Coding)
OOK	On-Off Keying
PA	Power Amplifier
PCB	Printed Circuit Board
PD	Power Down
PER	Packet Error Rate
PLL	Phase Locked Loop
POR	Power-On Reset
PQI	Preamble Quality Indicator
PTAT	Proportional To Absolute Temperature
QLP	Quad Leadless Package
QPSK	Quadrature Phase Shift Keying
RC	Resistor-Capacitor
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RX	Receive, Receive Mode
SMD	Surface Mount Device
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SRD	Short Range Devices
T/R	Transmit/Receive
TX	Transmit, Transmit Mode
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XTAL	Crystal

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1 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD + 0.3, max 3.9	V	
Voltage on the pins RF_P, RF_N, DCOUPL, RBIAS	–0.3	2.0	V	
Voltage ramp-up rate		120	kV/µs	
Input RF level		+10	dBm	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	According to IPC/JEDEC J-STD-020
ESD		750	V	According to JEDEC STD 22, method A114, Human Body Model (HBM)
ESD		400	V	According to JEDEC STD 22, C101C, Charged Device Model (CDM)

Table 1: Absolute Maximum Ratings

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

2 Operating Conditions

The operating conditions for **CC110L** are listed Table 2 in below.

Parameter	Min	Max	Unit	Condition
Operating temperature	–40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

3 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	300		348	MHz	
	387		464	MHz	If using a 27 MHz crystal, the lower frequency limit for this band is 392 MHz
	779		928	MHz	
Data rate	0.6		500	kBaud	2-FSK
	0.6		250	kBaud	GFSK and OOK
	0.6		300	kBaud	4-FSK (the data rate in kbps will be twice the baud rate)
					Optional Manchester encoding (the data rate in kbps will be half the baud rate)

Table 3: General Characteristics

4 Electrical Specifications

4.1 Current Consumption

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using [1] and [2]. Reduced current settings (`MDMCFG2.DEM_DCFILT_OFF=1`) gives a slightly lower current consumption at the cost of a reduction in sensitivity. See Table 7 for additional details on current consumption and sensitivity.

Parameter	Min	Typ	Max	Unit	Condition
Current consumption in power down modes		0.2	1	µA	Voltage regulator to digital part off, register values retained (SLEEP state). All GDO pins programmed to 0x2F (HW to 0)
		100		µA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with `MCSM0.OSC_FORCE_ON` set)
		165		µA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
Current consumption		1.7		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		8.4		mA	Only the frequency synthesizer is running (FSTXON state). This currents consumption is also representative for the other intermediate states when going from IDLE to RX or TX, including the calibration state
Current consumption, 315 MHz		15.4		mA	Receive mode, 1.2 kBaud, reduced current, input at sensitivity limit
		14.4		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		15.2		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit
		14.3		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		16.5		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.1		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		27.4		mA	Transmit mode, +10 dBm output power
		15.0		mA	Transmit mode, 0 dBm output power
		12.3		mA	Transmit mode, –6 dBm output power
Current consumption, 433 MHz		16.0		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.0		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		15.7		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.0		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		17.1		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit
		15.7		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit
		29.2		mA	Transmit mode, +10 dBm output power
		16.0		mA	Transmit mode, 0 dBm output power
		13.1		mA	Transmit mode, –6 dBm output power

Parameter	Min	Typ	Max	Unit	Condition
Current consumption, 868/915 MHz		15.7		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		14.7		mA	Receive mode, 1.2 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		15.6		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		14.6		mA	Receive mode, 38.4 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		16.9		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input at sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		15.6		mA	Receive mode, 250 kBaud, register settings optimized for reduced current, input well above sensitivity limit. See Figure 1 for current consumption with register settings optimized for sensitivity.
		34.2		mA	Transmit mode, +12 dBm output power, 868 MHz
		30.0		mA	Transmit mode, +10 dBm output power, 868 MHz
		16.8		mA	Transmit mode, 0 dBm output power, 868 MHz
		16.4		mA	Transmit mode, –6 dBm output power, 868 MHz.
		33.4		mA	Transmit mode, +11 dBm output power, 915 MHz
		30.7		mA	Transmit mode, +10 dBm output power, 915 MHz
		17.2		mA	Transmit mode, 0 dBm output power, 915 MHz
		17.0		mA	Transmit mode, –6 dBm output power, 915 MHz

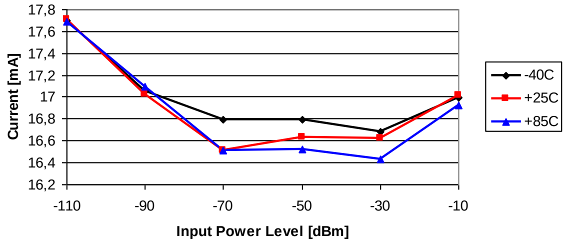
Table 4: Current Consumption

	Supply Voltage VDD = 1.8 V			**Supply Voltage VDD = 3.0 V**			**Supply Voltage VDD = 3.6 V**		
Temperature [°C]	−40	25	85	−40	25	85	−40	25	85
Current [mA], `PATABLE=0xC0`**, +12 dBm**	32.7	31.5	30.5	35.3	34.2	33.3	35.5	34.4	33.5
Current [mA], `PATABLE=0xC5`**, +10 dBm**	30.1	29.2	28.3	30.9	30.0	29.4	31.1	30.3	29.6
Current [mA], `PATABLE=0x50`**, 0 dBm**	16.4	16.0	15.6	17.3	16.8	16.4	17.6	17.1	16.7

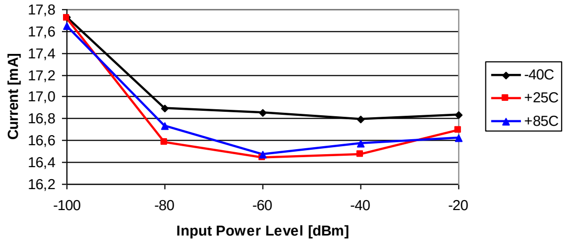
Table 5: Typical TX Current Consumption over Temperature and Supply Voltage, 868 MHz

	Supply Voltage VDD = 1.8 V			**Supply Voltage VDD = 3.0 V**			**Supply Voltage VDD = 3.6 V**		
Temperature [°C]	−40	25	85	−40	25	85	−40	25	85
Current [mA], `PATABLE=0xC0`**, +11 dBm**	31.9	30.7	29.8	34.6	33.4	32.5	34.8	33.6	32.7
Current [mA], `PATABLE=0xC3`**, +10 dBm**	30.9	29.8	28.9	31.7	30.7	30.0	31.9	31.0	30.2
Current [mA], `PATABLE=0x8E`**, 0 dBm**	17.2	16.8	16.4	17.6	17.2	16.9	17.8	17.4	17.1

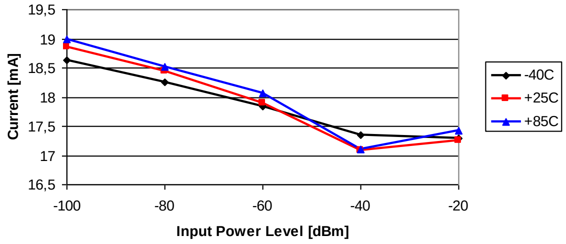
Table 6: Typical TX Current Consumption over Temperature and Supply Voltage, 915 MHz



1.2 kBaud GFSK



38.4 kBaud GFSK



250 kBaud GFSK

Figure 1: Typical RX Current Consumption over Temperature and Input Power Level, 868/915 MHz, Sensitivity Optimized Setting

4.2 RF Receive Section

T_A = 25°C, VDD = 3.0 V if nothing else stated. All measurement results are obtained using [1] and [2].

Parameter	Min	Typ	Max	Unit	Condition/Note
Digital channel filter bandwidth	58		812	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0 MHz crystal)
Spurious emissions		–68 –66	–57 –47	dBm dBm	25 MHz - 1 GHz (Maximum figure is the ETSI EN 300 220 V2.3.1 limit) Above 1 GHz (Maximum figure is the ETSI EN 300 220 V2.3.1 limit) Typical radiated spurious emission is –49 dBm measured at the VCO frequency
RX latency		9		bit	Serial operation. Time from start of reception until data is available on the receiver data output pin is equal to 9 bit
315 MHz					
1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (2-FSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–111		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.2 mA to 15.4 mA at the sensitivity limit. The sensitivity is typically reduced to -109 dBm
433 MHz					
1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–112		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 18.0 mA to 16.0 mA at the sensitivity limit. The sensitivity is typically reduced to –110 dBm
38.4 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		–104		dBm	
250 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		–95		dBm	
868/915 MHz					
1.2 kBaud data rate, sensitivity optimized, `MDMCFG2.DEM_DCFILT_OFF=0` (GFSK, 1% packet error rate, 20 bytes packet length, 5.2 kHz deviation, 58 kHz digital channel filter bandwidth)					
Receiver sensitivity		–112		dBm	Sensitivity can be traded for current consumption by setting `MDMCFG2.DEM_DCFILT_OFF=1`. The typical current consumption is then reduced from 17.7 mA to 15.7 mA at sensitivity limit. The sensitivity is typically reduced to –109 dBm
Saturation		–14		dBm	`FIFOTHR.CLOSE_IN_RX=0`. See more in DN010 [5]
Adjacent channel rejection ±100 kHz offset		37		dB	Desired channel 3 dB above the sensitivity limit. 100 kHz channel spacing See Figure 2 for selectivity performance at other offset frequencies
Image channel rejection		31		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 –50 –40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 2 for blocking performance at other offset frequencies

Parameter	Min	Typ	Max	Unit	Condition/Note
38.4 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (GFSK, 1% packet error rate, 20 bytes packet length, 20 kHz deviation, 100 kHz digital channel filter bandwidth)					
Receiver sensitivity		–104		dBm	Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced from 17.7 mA to 15.6 mA at the sensitivity limit. The sensitivity is typically reduced to -102 dBm
Saturation		–16		dBm	FIFOTHR.CLOSE_IN_RX=0. See more in DN010 [5]
Adjacent channel rejection –200 kHz offset +200 kHz offset		 12 25		 dB dB	Desired channel 3 dB above the sensitivity limit. 200 kHz channel spacing See Figure 3 for blocking performance at other offset frequencies
Image channel rejection		23		dB	IF frequency 152 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 –50 –40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 3 for blocking performance at other offset frequencies
250 kBaud data rate, sensitivity optimized, MDMCFG2.DEM_DCFILT_OFF=0 (GFSK, 1% packet error rate, 20 bytes packet length, 127 kHz deviation, 540 kHz digital channel filter bandwidth)					
Receiver sensitivity		–95		dBm	Sensitivity can be traded for current consumption by setting MDMCFG2.DEM_DCFILT_OFF=1. The typical current consumption is then reduced from 18.9 mA to 16.9 mA at the sensitivity limit. The sensitivity is typically reduced to -91 dBm
Saturation		–17		dBm	FIFOTHR.CLOSE_IN_RX=0. See more in DN010 [5]
Adjacent channel rejection		25		dB	Desired channel 3 dB above the sensitivity limit. 750 kHz channel spacing See Figure 4 for blocking performance at other offset frequencies
Image channel rejection		14		dB	IF frequency 304 kHz Desired channel 3 dB above the sensitivity limit
Blocking ±2 MHz offset ±10 MHz offset		 -50 -40		 dBm dBm	Desired channel 3 dB above the sensitivity limit See Figure 4 for blocking performance at other offset frequencies

Table 7: RF Receive Section

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	–40	25	85	–40	25	85	–40	25	85
Sensitivity [dBm] 1.2 kBaud	–113	–112	–110	–113	–112	–110	–113	–112	–110
Sensitivity [dBm] 38.4 kBaud	–105	–104	–102	–105	–104	–102	–105	–104	–102
Sensitivity [dBm] 250 kBaud	–97	–96	–92	–97	–95	–92	–97	–94	–92

Table 8: Typical Sensitivity over Temperature and Supply Voltage, 868 MHz, Sensitivity Optimized Setting

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	–40	25	85	–40	25	85	–40	25	85
Sensitivity [dBm] 1.2 kBaud	–113	–112	–110	–113	–112	–110	–113	–112	–110
Sensitivity [dBm] 38.4 kBaud	–105	–104	–102	–104	–104	–102	–105	–104	–102
Sensitivity [dBm] 250 kBaud	–97	–94	–92	–97	–95	–92	–97	–95	–92

Table 9: Typical Sensitivity over Temperature and Supply Voltage, 915 MHz, Sensitivity Optimized Setting

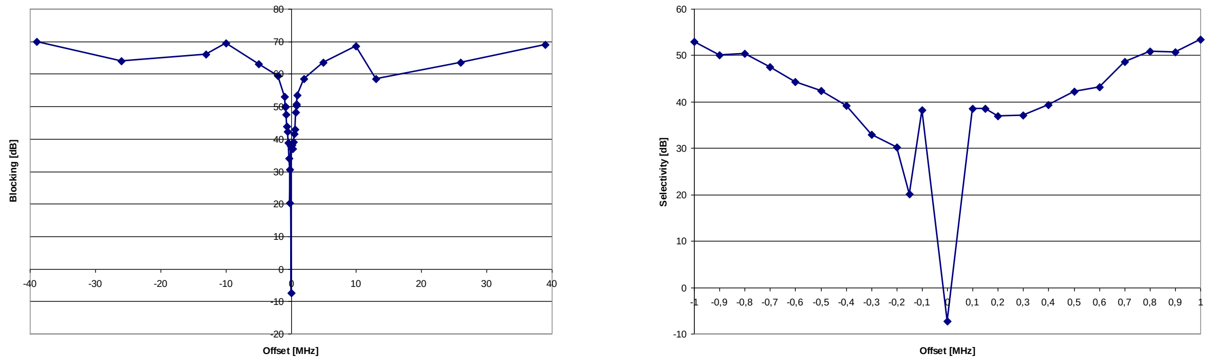


Figure 2: Typical Selectivity at 1.2 kBaud Data Rate, 868.3 MHz, GFSK, 5.2 kHz Deviation. IF Frequency is 152.3 kHz and the Digital Channel Filter Bandwidth is 58 kHz

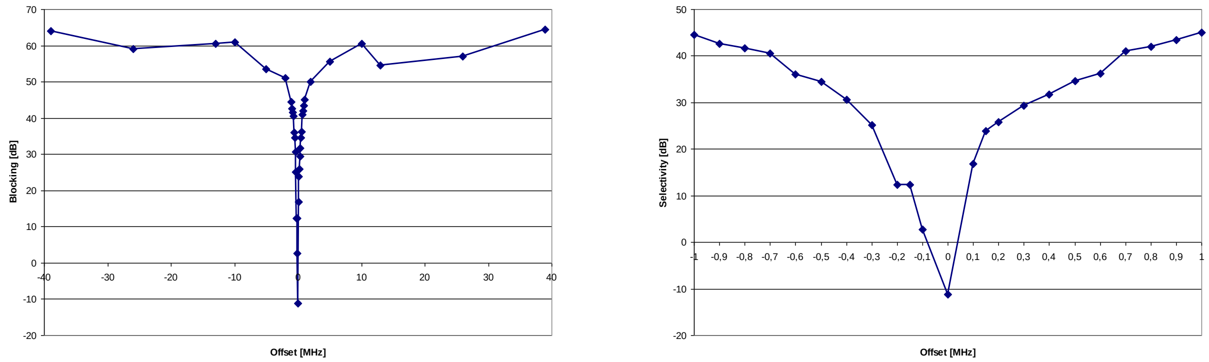


Figure 3: Typical Selectivity at 38.4 kBaud Data Rate, 868 MHz, GFSK, 20 kHz Deviation. IF Frequency is 152.3 kHz and the Digital Channel Filter Bandwidth is 100 kHz

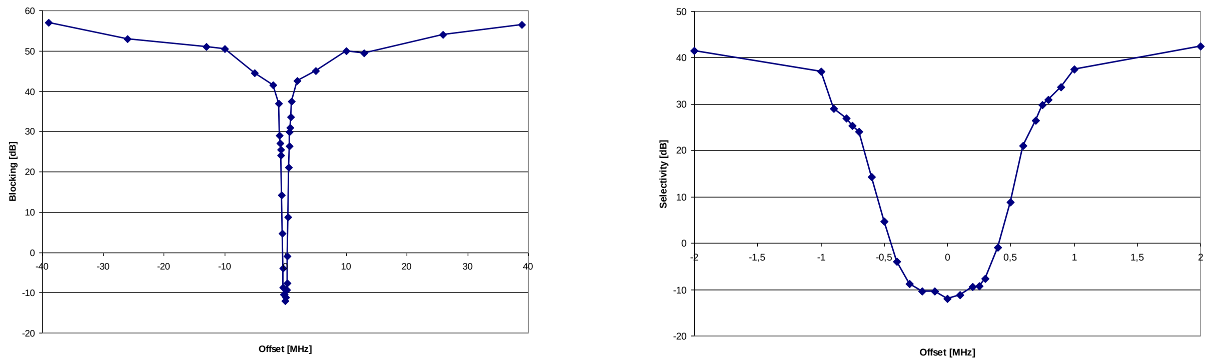


Figure 4: Typical Selectivity at 250 kBaud Data Rate, 868 MHz, GFSK, IF Frequency is 304 kHz and the Digital Channel Filter Bandwidth is 540 kHz

4.3 RF Transmit Section

T_A = 25°C, VDD = 3.0 V, +10 dBm if nothing else stated. All measurement results are obtained using [1] and [2].

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance					Differential impedance as seen from the RF-port (RF_P and RF_N) towards the antenna.
315 MHz		122 + j31		Ω	
433 MHz		116 + j41		Ω	
868/915 MHz		86.5 + j43		Ω	
Output power, highest setting					Output power is programmable, and full range is available in all frequency bands. Output power may be restricted by regulatory limits.
315 MHz		+10		dBm	See Design Note DN013 [10] for output power and harmonics figures when using *multi-layer* inductors. The output power is then typically +10 dBm when operating at 868/915 MHz.
433 MHz		+10		dBm	
868 MHz		+12		dBm	
915 MHz		+11		dBm	Delivered to a 50 Ω single-ended load via the RF matching network in [1] and [2]
Output power, lowest setting		−30		dBm	Output power is programmable, and full range is available in all frequency bands Delivered to a 50Ω single-ended load via the RF matching network in [1] and [2]
Harmonics, radiated					Measured on [1] and [2] with CW, maximum output power The antennas used during the radiated measurements (SMAFF-433 from R.W. Badland and Nearson S331 868/915) play a part in attenuating the harmonics
2^{nd} Harm, 433 MHz		−49		dBm	
3^{rd} Harm, 433 MHz		−40		dBm	
2^{nd} Harm, 868 MHz		−47		dBm	
3^{rd} Harm, 868 MHz		−55		dBm	
2^{nd} Harm, 915 MHz		−50		dBm	Note: All harmonics are below −41.2 dBm when operating in the 902 - 928 MHz band
3^{rd} Harm, 915 MHz		−54		dBm	
Harmonics, conducted					Measured with +10 dBm CW at 315 MHz and 433 MHz
315 MHz		< −35		dBm	Frequencies below 960 MHz
		< −53		dBm	Frequencies above 960 MHz
433 MHz		−43		dBm	Frequencies below 1 GHz
		< −45		dBm	Frequencies above 1 GHz
868 MHz					
2^{nd} Harm		−36		dBm	Measured with +12 dBm CW at 868 MHz
other harmonics		< −46		dBm	
915 MHz					
2^{nd} Harm		−34		dBm	Measured with +11 dBm CW at 915 MHz (requirement is −20 dBc under FCC 15.247)
other harmonics		< −50		dBm	

Parameter	Min	Typ	Max	Unit	Condition/Note
Spurious emissions conducted, harmonics not included					Measured with +10 dBm CW at 315 MHz and 433 MHz
315 MHz		< −58 < −53		dBm dBm	Frequencies below 960 MHz Frequencies above 960 MHz
433 MHz		< −50 < −54 < −56		dBm dBm dBm	Frequencies below 1 GHz Frequencies above 1 GHz Frequencies within 47-74, 87.5-118, 174-230, 470-862 MHz
868 MHz		< −50 < −52 < −53		dBm dBm dBm	Measured with +12 dBm CW at 868 MHz Frequencies below 1 GHz Frequencies above 1 GHz Frequencies within 47-74, 87.5-118, 174-230, 470-862 MHz All radiated spurious emissions are within the limits of ETSI. The peak conducted spurious emission is −53 dBm at 699 MHz (868 MHz - 169 MHz), which is in a frequency band limited to −54 dBm by EN 300 220 V2.3.1. An alternative filter can be used to reduce the emission at 699 MHz below −54 dBm, for conducted measurements, and is shown in Figure 8. See more information in DN017 [6]. For compliance with modulation bandwidth requirements under EN 300 220 V2.3.1 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz.
915 MHz		< −51 < −54		dBm dBm	Measured with +11 dBm CW at 915 MHz Frequencies below 960 MHz Frequencies above 960 MHz
TX latency		8		bit	Serial operation. Time from sampling the data on the transmitter data input pin until it is observed on the RF output ports

Table 10: RF Transmit Section

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	−40	25	85	−40	25	85	−40	25	85
Output Power [dBm], `PATABLE=0xC0`**, +12 dBm**	12	11	10	12	12	11	12	12	11
Output Power [dBm], `PATABLE=0xC5`**, +10 dBm**	11	10	9	11	10	10	11	10	10
Output Power [dBm], `PATABLE=0x50`**, 0 dBm**	1	0	-1	2	1	0	2	1	0

Table 11: Typical Variation in Output Power over Temperature and Supply Voltage, 868 MHz

	Supply Voltage VDD = 1.8 V			Supply Voltage VDD = 3.0 V			Supply Voltage VDD = 3.6 V		
Temperature [°C]	−40	25	85	−40	25	85	−40	25	85
Output Power [dBm], `PATABLE=0xC0`**, +11 dBm**	11	10	10	12	11	11	12	11	11
Output Power [dBm], `PATABLE=0x8E`**, +0 dBm**	2	1	0	2	1	0	2	1	0

Table 12: Typical Variation in Output Power over Temperature and Supply Voltage, 915 MHz

4.4 Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results obtained using [1] and [2].

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	27	MHz	For compliance with modulation bandwidth requirements under EN 300 220 V2.3.1 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz.
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) crystal loading, c) aging, and d) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
Load capacitance	10	13	20	pF	Simulated over operating conditions
ESR			100	Ω	
Start-up time		150		µs	This parameter is to a large degree crystal dependent. Measured on [1] and [2] using crystal AT-41CD2 from NDK

Table 13: Crystal Oscillator Parameters

4.5 Frequency Synthesizer Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else is stated. All measurement results are obtained using [1] and [2]. Min figures are given using a 27 MHz crystal. Typ and max figures are given using a 26 MHz crystal.

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{16}$	412	Hz	26 - 27 MHz crystal. The resolution (in Hz) is equal for all frequency bands
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing
RF carrier phase noise		–92		dBc/Hz	@ 50 kHz offset from carrier
RF carrier phase noise		–92		dBc/Hz	@ 100 kHz offset from carrier
RF carrier phase noise		–92		dBc/Hz	@ 200 kHz offset from carrier
RF carrier phase noise		–98		dBc/Hz	@ 500 kHz offset from carrier
RF carrier phase noise		–107		dBc/Hz	@ 1 MHz offset from carrier
RF carrier phase noise		–113		dBc/Hz	@ 2 MHz offset from carrier
RF carrier phase noise		–119		dBc/Hz	@ 5 MHz offset from carrier
RF carrier phase noise		–129		dBc/Hz	@ 10 MHz offset from carrier
PLL turn-on / hop time (See Table 29)	72	75	75	µs	Time from leaving the IDLE state until arriving in the RX, FSTXON or TX state, when not performing calibration. Crystal oscillator running.
PLL RX/TX settling time (See Table 29)	29	30	30	µs	Settling time for the 1·IF frequency step from RX to TX
PLL TX/RX settling time (See Table 29)	30	31	31	µs	Settling time for the 1·IF frequency step from TX to RX. 250 kbps data rate.
PLL calibration time (See Table 30)	685	712	724	µs	Calibration can be initiated manually or automatically before entering or after leaving RX/TX

Table 14: Frequency Synthesizer Parameters

4.6 DC Characteristics

T_A = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD – 0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4 mA output current
Logic "1" output voltage	VDD – 0.3	VDD	V	For up to 4 mA output current
Logic "0" input current	N/A	–50	nA	Input equals 0 V
Logic "1" input current	N/A	50	nA	Input equals VDD

Table 15: DC Characteristics

4.7 Power-On Reset

For proper Power-On-Reset functionality the power supply should comply with the requirements in Table 16 below. Otherwise, the chip should be assumed to have unknown state until transmitting an `SRES` strobe over the SPI interface. See Section 18.1 on page 40 for further details.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power-up ramp-up time			5	ms	From 0V until reaching 1.8V
Power off time	1			ms	Minimum time between power-on and power-off

Table 16: Power-On Reset Requirements

5 Pin Configuration

The CC110L pin-out is shown in Figure 5 and Table 17. See Section 24 for details on the I/O configuration.

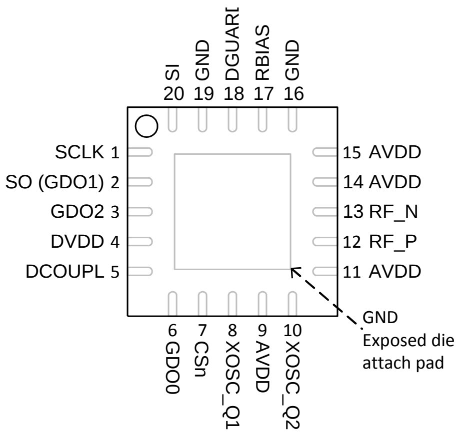


Figure 5: Pinout Top View

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip

Pin #	Pin Name	Pin type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input
2	SO (GDO1)	Digital Output	Serial configuration interface, data output Optional general output pin when CSn is high
3	GDO2	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clear channel indicator • Clock output, down-divided from XOSC • Serial output RX data
4	DVDD	Power (Digital)	1.8 - 3.6 V digital power supply for digital I/O's and for the digital core voltage regulator
5	DCOUPL	Power (Digital)	1.6 - 2.0 V digital power supply output for decoupling **NOTE:** This pin is intended for use with the CC110L only. It can not be used to provide supply voltage to other devices
6	GDO0	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clear channel indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data
7	CSn	Digital Input	Serial configuration interface, chip select
8	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
9	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
10	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
11	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
12	RF_P	RF I/O	Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode
13	RF_N	RF I/O	Negative RF input signal to LNA in receive mode Negative RF output signal from PA in transmit mode
14	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
15	AVDD	Power (Analog)	1.8 - 3.6 V analog power supply connection
16	GND	Ground (Analog)	Analog ground connection
17	RBIAS	Analog I/O	External bias resistor for reference current
18	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
19	GND	Ground (Digital)	Ground connection for digital noise isolation
20	SI	Digital Input	Serial configuration interface, data input

Table 17: Pinout Overview

6 Circuit Description

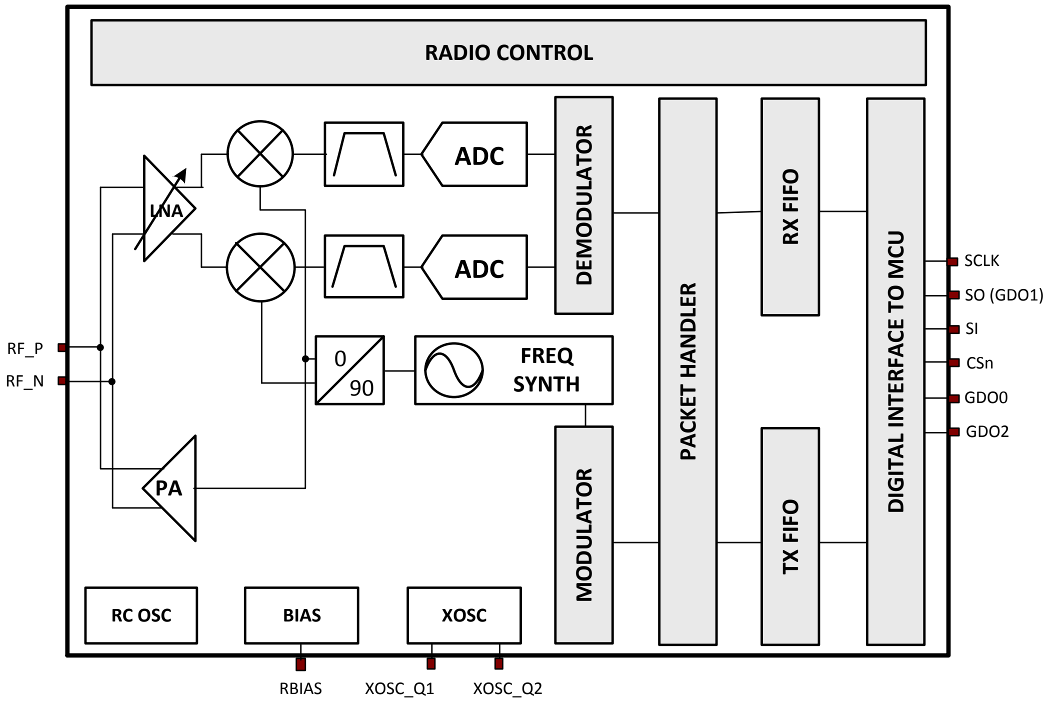


Figure 6: CC110L Simplified Block Diagram

A simplified block diagram of CC110L is shown in Figure 6.

CC110l features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitised by the ADCs. Automatic gain control (AGC), fine channel filtering, demodulation, and bit/packet synchronization are performed digitally.

The transmitter part of CC110L is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90 degree phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling, and data buffering.

7 Application Circuit

The low cost application circuits ([17] and [18]), which use multi layer inductors, are shown in Figure 7 and Figure 8 (see Table 18 for component values).

The designs in [1] and [2] were used for CC110L characterization. The 315 MHz and 433 MHz design [1] use inexpensive multi-layer inductors similar to the low cost application circuit while the 868 MHz and 915 MHz design [2] use wire-wound inductors. Wire-wound inductors give better output power and attenuation of harmonics compared to using multi-layer inductors.

Refer to design note DN032 [16] for information about performance when using wire-wound inductors from different vendors. See also Design Note DN013 [10], which gives the output power and harmonics when using *multi-layer* inductors. The output power is then typically +10 dBm when operating at 868/915 MHz.

7.1 Bias Resistor

The 56 kΩ bias resistor R171 is used to set an accurate bias current.

7.2 Balun and RF Matching

The balun and LC filter component values and their placement are important to keep the performance optimized. Gerber files and schematics for the reference designs are available for download from the TI website

The components between the RF_N/RF_P pins and the point where the two signals are joined together (C131, C122, L122, and L132 in Figure 7 and L121, L131, C121, L122, C131, C122, and L132 in Figure 8) form a balun that converts the differential RF signal on CC110L to a single-ended RF signal. C124 is needed for DC blocking.

L123, L124, and C123 (plus C125 in Figure 7) form a low-pass filter for harmonics attenuation.

The balun and LC filter components also matches the CC110L input impedance to a 50 Ω load. C126 provides DC blocking and is only needed if there is a DC path in the antenna. For the application circuit in Figure 8, this component may also be used for additional filtering, see Section 7.5.

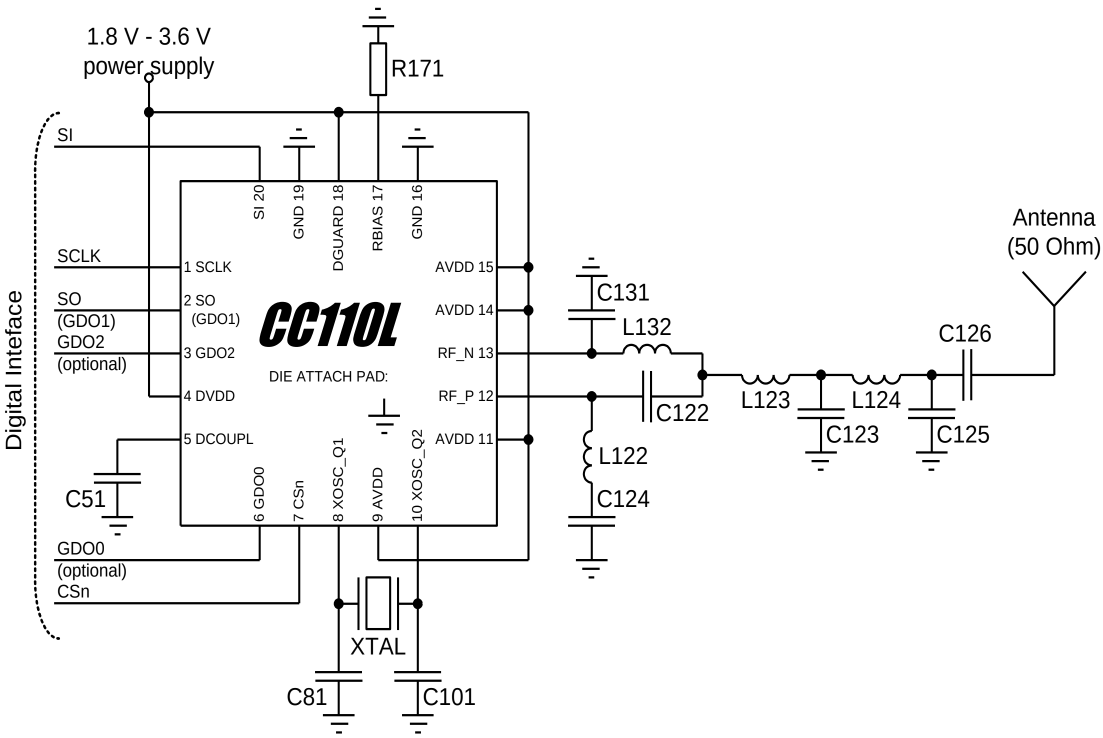


Figure 7: Typical Application and Evaluation Circuit 315/433 MHz (excluding supply decoupling capacitors)

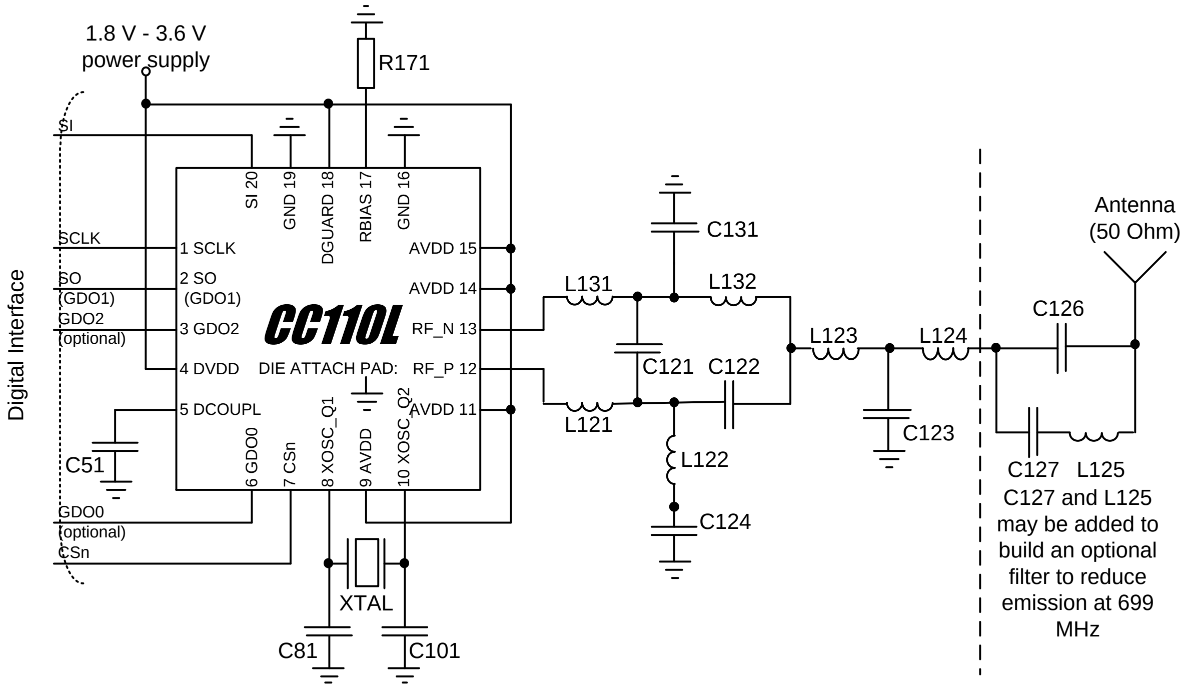


Figure 8: Typical Application and Evaluation Circuit 868/915 MHz (excluding supply decoupling capacitors)

Component	Value at 315 MHz	Value at 433 MHz	Value at 868/915 MHz	
			Without C127 and L125	With C127 and L125
C121			1 pF	1 pF
C122	6.8 pF	3.9 pF	1.5 pF	1.5 pF
C123	12 pF	8.2 pF	3.3 pF	3.3 pF
C124	220 pF	220 pF	100 pF	100 pF
C125	6.8 pF	5.6 pF		
C126	220 pF	220 pF	100 pF	12 pF
C127				47 pF
C131	6.8 pF	3.9 pF	1.5 pF	1.5 pF
L121			12 nH	12 nH
L122	33 nH	27 nH	18 nH	18 nH
L123	18 nH	22 nH	12 nH	12 nH
L124	33 nH	27 nH	12 nH	12 nH
L125				3.3 nH
L131			12 nH	12 nH
L132	33 nH	27 nH	18 nH	18 nH

Table 18: External Components

7.3 Crystal

A crystal in the frequency range 26 - 27 MHz must be connected between the XOSC_Q1 and XOSC_Q2 pins. The oscillator is designed for parallel mode operation of the crystal. In addition, loading capacitors (C81 and C101) for the crystal are required. The loading capacitor values depend on the total load capacitance, C_L, specified for the crystal. The total load capacitance seen between the crystal terminals should equal C_L for the crystal to oscillate at the specified frequency.

$$C_L = \frac{1}{\frac{1}{C_{81}} + \frac{1}{C_{101}}} + C_{parasitic}$$

The parasitic capacitance is constituted by pin input capacitance and PCB stray capacitance. Total parasitic capacitance is typically 2.5 pF.

The crystal oscillator is amplitude regulated. This means that a high current is used to start up the oscillations. When the amplitude builds up, the current is reduced to what is necessary to maintain approximately 0.4 Vpp signal swing. This ensures a fast start-up, and keeps the drive level to a minimum. The ESR of the crystal should be within the specification in order to ensure a reliable start-up (see Section 4.4 on page 14).

The initial tolerance, temperature drift, aging and load pulling should be carefully specified in order to meet the required frequency accuracy in a certain application.

Avoid routing digital signals with sharp edges close to XOSC_Q1 PCB track or underneath the crystal Q1 pad as this may shift the crystal dc operating point and result in duty cycle variation.

For compliance with modulation bandwidth requirements under EN 300 220 V2.3.1 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz.

7.4 Reference Signal

The chip can alternatively be operated with a reference signal from 26 to 27 MHz instead of a crystal. This input clock can either be a full-swing digital signal (0 V to VDD) or a sine wave of maximum 1 V peak-peak amplitude. The reference signal must be connected to the XOSC_Q1 input. The sine wave must be connected to XOSC_Q1 using a serial capacitor. When using a full-swing digital signal, this capacitor can be omitted. The XOSC_Q2 line must be left un-connected. C81 and C101 can be omitted when using a reference signal.

7.5 Additional Filtering

In the 868/915 MHz reference design [18], C127 and L125 together with C126 build an optional filter to reduce emission at carrier frequency - 169 MHz. This filter is necessary for applications with an external antenna connector that seek compliance with ETSI EN 300 220 V2.3.1. For more information, see DN017 [6].

If this filtering is not necessary, C126 will work as a DC block (only necessary if there is a DC path in the antenna). C127 and L125 should in that case be left unmounted.

Additional external components (e.g. an RF SAW filter) may be used in order to improve the performance in specific applications.

7.6 Power Supply Decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance ([17] and [18] should be followed closely).

7.7 PCB Layout Recommendations

The top layer should be used for signal routing, and the open areas should be filled with metallization connected to ground using several vias.

The area under the chip is used for grounding and shall be connected to the bottom ground plane with several vias for good thermal performance and sufficiently low inductance to ground.

In [17] and [18], 5 vias are placed inside the exposed die attached pad. These vias should be "tented" (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process.

The solder paste coverage should not be 100%. If it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Using "tented" vias reduces the solder paste coverage below 100%. See Figure 9 for top solder resist and top paste masks.

Each decoupling capacitor should be placed as close as possible to the supply pin it is supposed to decouple. Each decoupling capacitor should be connected to the power line (or power plane) by separate vias. The best routing is from the power line (or power plane) to the decoupling capacitor and then to the CC110L supply pin. Supply power filtering is very important.

Each decoupling capacitor ground pad should be connected to the ground plane by separate vias. Direct connections between neighboring power pins will increase noise coupling and should be avoided unless absolutely necessary. Routing in the ground plane underneath the chip or the balun/RF matching circuit, or between the chip's ground vias and the decoupling capacitor's ground vias should be avoided. This improves the grounding and ensures the shortest possible current return path.

Avoid routing digital signals with sharp edges close to XOSC_Q1 PCB track or underneath the crystal Q1 pad as this may shift the crystal dc operating point and result in duty cycle variation.

The external components should ideally be as small as possible (0402 is recommended) and surface mount devices are highly recommended. Please note that components with different sizes than those specified may have differing characteristics.

Precaution should be used when placing the microcontroller in order to avoid noise interfering with the RF circuitry.

A CC11xL Development Kit with a fully assembled CC110L Evaluation Module is available. It is strongly advised that this reference layout is followed very closely in order to get the best performance. The schematic, BOM and layout Gerber files are all available from the TI website ([17] and [18]).

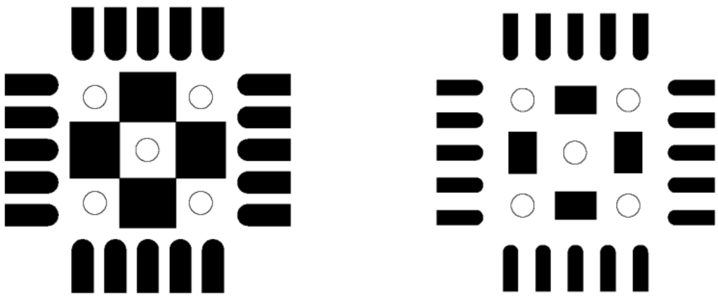


Figure 9: Left: Top Solder Resist Mask (Negative). Right: Top Paste Mask. Circles are Vias

8 Configuration Overview

CC110L can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. See Section 10 for more description of the SPI interface. The following key parameters can be programmed:

- Power-down / power up mode
- Crystal oscillator power-up / power-down
- Receive / transmit mode
- Carrier frequency / RF channel
- Data rate
- Modulation format
- RX channel filter bandwidth
- RF output power
- Data buffering with separate 64-byte RX and TX FIFOs
- Packet radio hardware support

Details of each configuration register can be found in Section 27, starting on page 52.

Figure 10 shows a simplified state diagram that explains the main CC110L states together with typical usage and current consumption. For detailed information on controlling the

CC110L state machine, and a complete state diagram, see Section 18, starting on page 39.

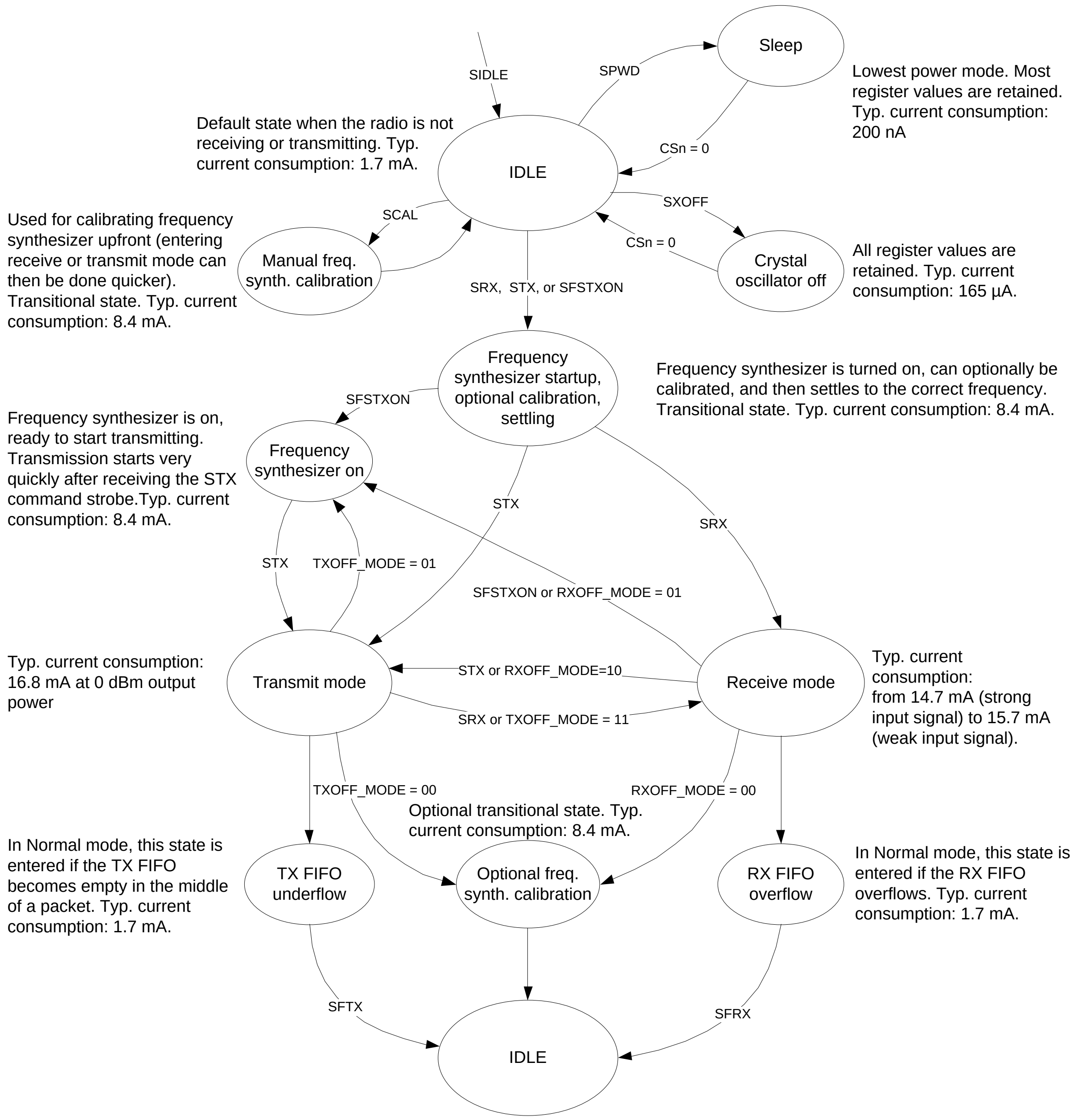


Figure 10: Simplified Radio Control State Diagram, with Typical Current Consumption at 1.2 kBaud Data Rate and `MDMCFG2.DEM_DCFILT_OFF=1` (current optimized). Frequency Band = 868 MHz

9 Configuration Software

CC110L can be configured using the SmartRF™ Studio software [4]. The SmartRF Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality.

After chip reset, all the registers have default values as shown in the tables in Section 27. The optimum register setting might differ from the default value. After a reset all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

10 4-wire Serial Configuration and Data Interface

CC110L is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK and CSn) where CC110L is the slave. This interface is also used to read and write buffered data. All transfers on the SPI interface are done most significant bit first.

All transactions on the SPI interface start with a header byte containing a R/$\overline{W}$ bit, a burst access bit (B), and a 6-bit address (A_5 - A_0).

The CSn pin must be kept low during transfers on the SPI bus. If CSn goes high during the transfer of a header byte or during read/write from/to a register, the transfer will be cancelled. The timing for the address and data transfer on the SPI interface is shown in Figure 11 with reference to Table 19.

When CSn is pulled low, the MCU must wait until CC110L SO pin goes low before starting to transfer the header byte. This indicates that the crystal is running. Unless the chip was in the SLEEP or XOFF states, the SO pin will always go low immediately after taking CSn low.

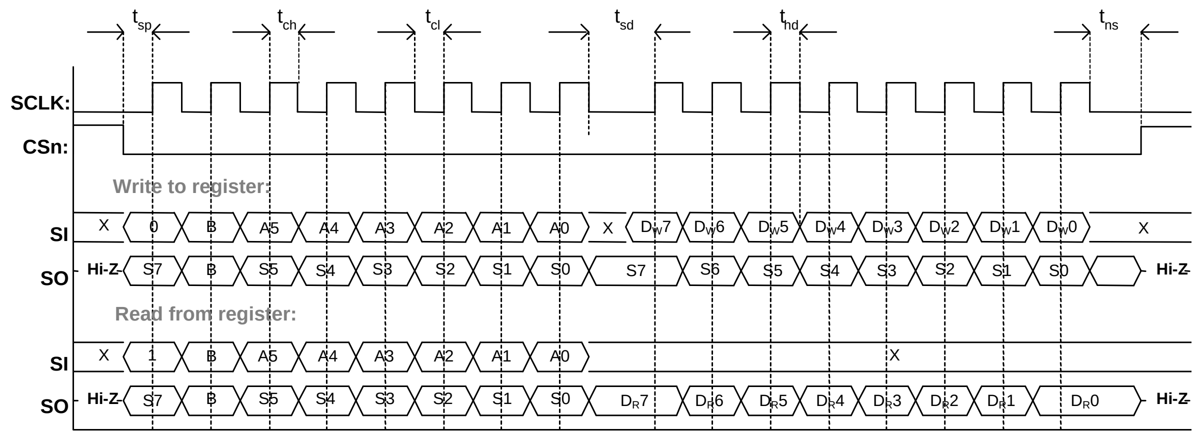


Figure 11: Configuration Registers Write and Read Operations

Parameter	Description		Min	Max	Units
f_{SCLK}	SCLK frequency 100 ns delay inserted between address byte and data byte (single access), or between address and data, and between each data byte (burst access).		-	10	MHz
	SCLK frequency, single access No delay between address and data byte		-	9	
	SCLK frequency, burst access No delay between address and data byte, or between data bytes		-	6.5	
$t_{sp,pd}$	CSn low to positive edge on SCLK, in power-down mode		150	-	μs
t_{sp}	CSn low to positive edge on SCLK, in active mode		20	-	ns
t_{ch}	Clock high		50	-	ns
t_{cl}	Clock low		50	-	ns
t_{rise}	Clock rise time		-	40	ns
t_{fall}	Clock fall time		-	40	ns
t_{sd}	Setup data (negative SCLK edge) to positive edge on SCLK (t_{sd} applies between address and data bytes, and between data bytes)	Single access	55	-	ns
		Burst access	76	-	
t_{hd}	Hold data after positive edge on SCLK		20	-	ns
t_{ns}	Negative edge on SCLK to CSn high.		20	-	ns

Table 19: SPI Interface Timing Requirements

Note: The minimum $t_{sp,pd}$ figure in Table 19 can be used in cases where the user does not read the `CHIP_RDYn` signal. CSn low to positive edge on SCLK when the chip is woken from power-down depends on the start-up time of the crystal being used. The 150 µs in Table 19 is the crystal oscillator start-up time measured on [1] and [2] using crystal AT-41CD2 from NDK.

10.1 Chip Status Byte

When the header byte, data byte, or command strobe is sent on the SPI interface, the chip status byte is sent by the CC110L on the SO pin. The status byte contains key status signals, useful for the MCU. The first bit, s7, is the `CHIP_RDYn` signal and this signal must go low before the first positive edge of SCLK. The `CHIP_RDYn` signal indicates that the crystal is running.

Bits 6, 5, and 4 comprise the `STATE` value. This value reflects the state of the chip. The XOSC and power to the digital core are on in the IDLE state, but all other modules are in power down. The frequency and channel configuration should only be updated when the chip is in this state. The RX state will be active when the chip is in receive mode. Likewise, TX is active when the chip is transmitting.

The last four bits (3:0) in the status byte contains `FIFO_BYTES_AVAILABLE`. For read operations (the R/$\overline{W}$ bit in the header byte is set to 1), the `FIFO_BYTES_AVAILABLE` field contains the number of bytes available for reading from the RX FIFO. For write operations (the R/$\overline{W}$ bit in the header byte is set to 0), the `FIFO_BYTES_AVAILABLE` field contains the number of bytes that can be written to the TX FIFO. When `FIFO_BYTES_AVAILABLE=15`, 15 or more bytes are available/free.

Table 20 gives a status byte summary.

<table>
<tr><th>Bits</th><th>Name</th><th colspan="3">Description</th></tr>
<tr><td>7</td><td>CHIP_RDYn</td><td colspan="3">Stays high until power and crystal have stabilized. Should always be low when using the SPI interface.</td></tr>
<tr><td rowspan="10">6:4</td><td rowspan="10">STATE[2:0]</td><td colspan="3">Indicates the current main state machine mode</td></tr>
<tr><td>Value</td><td>State</td><td>Description</td></tr>
<tr><td>000</td><td>IDLE</td><td>IDLE state
(Also reported for some transitional states instead of SETTLING or CALIBRATE)</td></tr>
<tr><td>001</td><td>RX</td><td>Receive mode</td></tr>
<tr><td>010</td><td>TX</td><td>Transmit mode</td></tr>
<tr><td>011</td><td>FSTXON</td><td>Fast TX ready</td></tr>
<tr><td>100</td><td>CALIBRATE</td><td>Frequency synthesizer calibration is running</td></tr>
<tr><td>101</td><td>SETTLING</td><td>PLL is settling</td></tr>
<tr><td>110</td><td>RXFIFO_OVERFLOW</td><td>RX FIFO has overflowed. Read out any useful data, then flush the FIFO with SFRX</td></tr>
<tr><td>111</td><td>TXFIFO_UNDERFLOW</td><td>TX FIFO has underflowed. Acknowledge with SFTX</td></tr>
<tr><td>3:0</td><td>FIFO_BYTES_AVAILABLE[3:0]</td><td colspan="3">The number of bytes available in the RX FIFO or free bytes in the TX FIFO</td></tr>
</table>

Table 20: Status Byte Summary

10.2 Register Access

The configuration registers on the CC110L are located on SPI addresses from 0x00 to 0x2E. Table 38 on page 54 lists all configuration registers. It is highly recommended to use SmartRF Studio [4] to generate optimum register settings. The detailed description of each register is found in Section 27.1 and 27.2, starting on page 57. All configuration registers can be both written to and read. The R/$\overline{W}$ bit controls if the register should be written to or read. When writing to registers, the status byte is sent on the SO pin each time a header byte or data byte is transmitted on the SI pin. When reading from registers, the status byte is sent on the SO pin each time a header byte is transmitted on the SI pin.

Registers with consecutive addresses can be accessed in an efficient way by setting the burst bit (B) in the header byte. The address bits (A_5 - A_0) set the start address in an internal address counter. This counter is incremented by one each new byte (every 8 clock pulses). The burst access is either a read or a write access and must be terminated by setting CSn high.

For register addresses in the range 0x30 - 0x3D, the burst bit is used to select between status registers when burst bit is one, and between command strobes when burst bit is zero. See more in Section 10.3 below. Because of this, burst access is not available for status registers and they must be accessed one at a time. The status registers can only be read.

10.3 SPI Read

When reading register fields over the SPI interface while the register fields are updated by the radio hardware (e.g. `MARCSTATE` or `TXBYTES`), there is a small, but finite, probability that a single read from the register is being corrupt. As an example, the probability of any single read from `TXBYTES` being corrupt, assuming the maximum data rate is used, is approximately 80 ppm. Refer to the CC110L Errata Notes [3] for more details.

10.4 Command Strobes

Command Strobes may be viewed as single byte instructions to CC110L. By addressing a command strobe register, internal sequences will be started. These commands are used to disable the crystal oscillator, enable receive mode, enable calibration etc. The 11 command strobes are listed in Table 37 on page 53.

> **Note:** An SIDLE strobe will clear all pending command strobes until IDLE state is reached. This means that if for example an SIDLE strobe is issued while the radio is in RX state, any other command strobes issued before the radio reaches IDLE state will be ignored.

The command strobe registers are accessed by transferring a single header byte (no data is being transferred). That is, only the R/$\overline{\text{W}}$ bit, the burst access bit (set to 0), and the six address bits (in the range 0x30 through 0x3D) are written. The R/$\overline{\text{W}}$ bit can be either one or zero and will determine how the `FIFO_BYTES_AVAILABLE` field in the status byte should be interpreted.

When writing command strobes, the status byte is sent on the SO pin.

A command strobe may be followed by any other SPI access without pulling CSn high. However, if an `SRES` strobe is being issued, one will have to wait for SO to go low again before the next header byte can be issued as shown in Figure 12. The command strobes are executed immediately, with the exception of the `SPWD` and the `SXOFF` strobes, which are executed when CSn goes high.

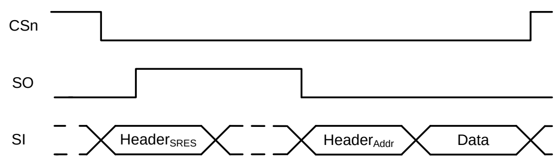


Figure 12: SRES Command Strobe

10.5 FIFO Access

The 64-byte TX FIFO and the 64-byte RX FIFO are accessed through the 0x3F address. When the R/$\overline{\text{W}}$ bit is zero, the TX FIFO is accessed, and the RX FIFO is accessed when the R/$\overline{\text{W}}$ bit is one.

The TX FIFO is write-only, while the RX FIFO is read-only.

The burst bit is used to determine if the FIFO access is a single byte access or a burst access. The single byte access method expects a header byte with the burst bit set to zero and one data byte. After the data byte, a new header byte is expected; hence, CSn can remain low. The burst access method expects one header byte and then consecutive data bytes until terminating the access by setting CSn high.

The following header bytes access the FIFOs:

- 0x3F: Single byte access to TX FIFO
- 0x7F: Burst access to TX FIFO
- 0xBF: Single byte access to RX FIFO
- 0xFF: Burst access to RX FIFO

When writing to the TX FIFO, the status byte (see Section 10.1) is output on SO for each new data byte as shown in Figure 11. This status byte can be used to detect TX FIFO underflow while writing data to the TX FIFO. Note that the status byte contains the number of bytes free before writing the byte in progress to the TX FIFO. When the last byte that fits in the TX FIFO is transmitted on SI, the status byte received concurrently on SO will indicate that one byte is free in the TX FIFO.

The TX FIFO may be flushed by issuing a `SFTX` command strobe. Similarly, a `SFRX` command strobe will flush the RX FIFO. A `SFTX` or `SFRX` command strobe can only be issued in the IDLE, TXFIFO_UNDERFLOW, or RXFIFO_OVERFLOW states. Both FIFOs are flushed when going to the SLEEP state.

Figure 13 gives a brief overview of different register access types possible.

10.6 PATABLE Access

The 0x3E address is used to access the `PATABLE`, which is used for selecting PA power control settings. The SPI expects one or two data bytes after receiving the address (the burst bit must be set if two bytes are to be written). For OOK, two bytes should be written to `PATABLE`; the first byte after the address will set the logic 0 power level and the second byte written will set the logic 1 power level. For all other modulations formats, only one byte should be written to `PATABLE`. Use SmartRF Studio [4] or DN013 [10] for recommended register values for a given output power.

The `PATABLE` can also be read by setting the R/$\overline{W}$ bit to 1. The read operation can be done as a single byte or burst access, depending on how many bytes should be read (one or two). Note that pulling CSn high will reset the index counter to zero, meaning that burst access needs to be used for reading/writing the second `PATABLE` entry. For the same reason, if one byte is written to the `PATABLE` and this value is to be read out, CSn must be set high before the read access in order to set the index counter back to zero.

Note that the content of the `PATABLE` is lost when entering the SLEEP state, except for the first byte, meaning that if OOK is used, the `PATABLE` needs to be reprogrammed when waking up from SLEEP.

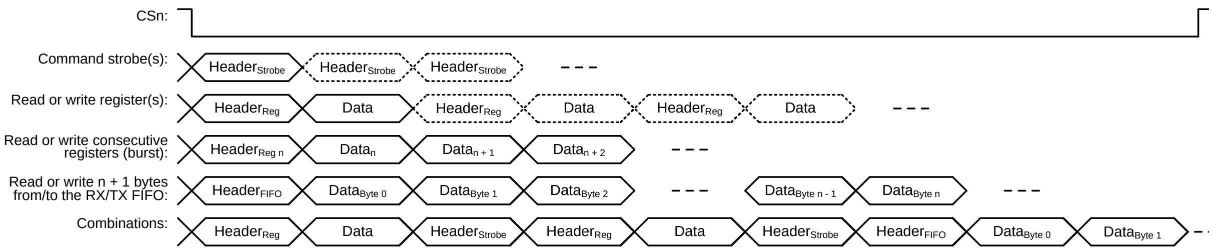


Figure 13: Register Access Types

11 Microcontroller Interface and Pin Configuration

In a typical system, **CC110L** will interface to a microcontroller. This microcontroller must be able to:

- Program **CC110L** into different modes
- Read and write buffered data
- Read back status information via the 4-wire SPI-bus configuration interface (SI, SO, SCLK and CSn)

11.1 Configuration Interface

The microcontroller uses four I/O pins for the SPI configuration interface (SI, SO, SCLK and CSn). The SPI is described in Section 10 on page 23.

11.2 General Control and Status Pins

The **CC110L** has two dedicated configurable pins (GDO0 and GDO2) and one shared pin (GDO1) that can output internal status information useful for control software. These pins can be used to generate interrupts on the MCU. See Section 24 on page 47 for more details on the signals that can be programmed.

GDO1 is shared with the SO pin in the SPI interface. The default setting for GDO1/SO is 3-state output. By selecting any other of the programming options, the GDO1/SO pin will become a generic pin. When CSn is low, the pin will always function as a normal SO pin.

In the synchronous and asynchronous serial modes, the GDO0 pin is used as a serial TX data input pin while in transmit mode.

12 Data Rate Programming

The data rate used when transmitting, or the data rate expected in receive is programmed by the `MDMCFG3.DRATE_M` and the `MDMCFG4.DRATE_E` configuration registers. The data rate is given by the formula below. As the formula shows, the programmed data rate depends on the crystal frequency.

$$R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$$

The following approach can be used to find suitable values for a given data rate:

$$DRATE\_E = \log_2\left(\frac{R_{DATA} \cdot 2^{20}}{f_{XOSC}}\right)$$

$$DRATE\_M = \frac{R_{DATA} \cdot 2^{28}}{f_{XOSC} \cdot 2^{DRATE\_E}} - 256$$

If `DRATE_M` is rounded to the nearest integer and becomes 256, increment `DRATE_E` and use `DRATE_M` = 0.

The data rate can be set from 0.6 kBaud to 500 kBaud with the minimum step size according to Table 21 below. See Table 3 for the minimum and maximum data rates for the different modulation formats.

Min Data Rate [kBaud]	Typical Data Rate [kBaud]	Max Data Rate [kBaud]	Data rate Step Size [kBaud]
0.6	1.0	0.79	0.0015
0.79	1.2	1.58	0.0031
1.59	2.4	3.17	0.0062
3.17	4.8	6.33	0.0124
6.35	9.6	12.7	0.0248
12.7	19.6	25.3	0.0496
25.4	38.4	50.7	0.0992
50.8	76.8	101.4	0.1984
101.6	153.6	202.8	0.3967
203.1	250	405.5	0.7935
406.3	500	500	1.5869

Table 21: Data Rate Step Size (assuming a 26 MHz crystal)

13 Receiver Channel Filter Bandwidth

In order to meet different channel width requirements, the receiver channel filter is programmable. The MDMCFG4.CHANBW_E and MDMCFG4.CHANBW_M configuration registers control the receiver channel filter bandwidth, which scales with the crystal oscillator frequency.

The following formula gives the relation between the register settings and the channel filter bandwidth:

$$BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$$

Table 22 lists the channel filter bandwidths supported by the CC110L.

MDMCFG4. CHANBW_M	MDMCFG4.CHANBW_E			
	00	**01**	**10**	**11**
00	812	406	203	102
01	650	325	162	81
10	541	270	135	68
11	464	232	116	58

Table 22: Channel Filter Bandwidths [kHz] (assuming a 26 MHz crystal)

For best performance, the channel filter bandwidth should be selected so that the signal bandwidth occupies at most 80% of the channel filter bandwidth. The channel centre tolerance due to crystal inaccuracy should also be subtracted from the channel filter bandwidth. The following example illustrates this:

With the channel filter bandwidth set to 500 kHz, the signal should stay within 80% of 500 kHz, which is 400 kHz. Assuming 915 MHz frequency and ±20 ppm frequency uncertainty for both the transmitting device and the receiving device, the total frequency uncertainty is ±40 ppm of 915 MHz, which is ±37 kHz. If the whole transmitted signal bandwidth is to be received within 400 kHz, the transmitted signal bandwidth should be maximum 400 kHz - 2·37 kHz, which is 326 kHz.

By compensating for a frequency offset between the transmitter and the receiver, the filter bandwidth can be reduced and the sensitivity can be improved, see more in DN005 [12] and in Section 14.1.

14 Demodulator, Symbol Synchronizer, and Data Decision

CC110L contains an advanced and highly configurable demodulator. Channel filtering and frequency offset compensation is performed digitally. To generate the RSSI level (see Section 17.2 for more information), the signal level in the channel is estimated. Data filtering is also included for enhanced performance.

14.1 Frequency Offset Compensation

The CC110L has a very fine frequency resolution (see Table 14). This feature can be used to compensate for frequency offset and drift.

When using 2-FSK, GFSK, or 4-FSK modulation, the demodulator will compensate for the offset between the transmitter and receiver frequency within certain limits, by estimating the centre of the received data. The frequency offset compensation configuration is controlled from the FOCCFG register. By compensating for a large frequency offset between the transmitter and the receiver, the sensitivity can be improved, see DN005 [12].

The tracking range of the algorithm is selectable as fractions of the channel bandwidth with the FOCCFG.FOC_LIMIT configuration register.

If the FOCCFG.FOC_BS_CS_GATE bit is set, the offset compensator will freeze until carrier sense asserts. This may be useful when the radio is in RX for long periods with no traffic, since the algorithm may drift to the boundaries when trying to track noise.

The tracking loop has two gain factors, which affects the settling time and noise sensitivity of the algorithm. FOCCFG.FOC_PRE_K sets the gain before the sync word is detected, and FOCCFG.FOC_POST_K selects the gain after the sync word has been found.

Note: Frequency offset compensation is not supported for OOK modulation.

The estimated frequency offset value is available in the FREQEST status register. This can be used for permanent frequency offset compensation. By writing the value from FREQEST into FSCTRL0.FREQOFF, the frequency synthesizer will automatically be adjusted according to the estimated frequency offset. More details regarding this permanent frequency compensation algorithm can be found in DN015 [7].

14.2 Bit Synchronization

The bit synchronization algorithm extracts the clock from the incoming symbols. The algorithm requires that the expected data rate is programmed as described in Section 12 on page 28. Re-synchronization is performed continuously to adjust for error in the incoming symbol rate.

14.3 Byte Synchronization

Byte synchronization is achieved by a continuous sync word search. The sync word is a 16 bit configurable field (can be repeated to get a 32 bit) that is automatically inserted at the start of the packet by the modulator in transmit mode. The MSB in the sync word is sent first. The demodulator uses this field to find the byte boundaries in the stream of bits. The sync word will also function as a system identifier, since only packets with the correct predefined sync word will be received if the sync word detection in RX is enabled in register MDMCFG2 (see Section 17.1). The sync word detector correlates against the user-configured 16 or 32 bit sync word. The correlation threshold can be set to 15/16, 16/16, or 30/32 bits match. The sync word can be further qualified using the preamble quality indicator mechanism described below and/or a carrier sense condition. The sync word is configured through the SYNC1 and SYNC0 registers.

15 Packet Handling Hardware Support

The CC110L has built-in hardware support for packet oriented radio protocols.

In transmit mode, the packet handler can be configured to add the following elements to the packet stored in the TX FIFO:

- A programmable number of preamble bytes
- A two byte synchronization (sync) word. Can be duplicated to give a 4-byte sync word (recommended). It is not possible to only insert preamble or only insert a sync word
- A CRC checksum computed over the data field.
- The recommended setting is 4-byte preamble and 4-byte sync word, except for 500 kBaud data rate where the recommended preamble length is 8 bytes.

In receive mode, the packet handling support will de-construct the data packet by implementing the following (if enabled):

- Preamble detection
- Sync word detection
- CRC computation and CRC check
- One byte address check
- Packet length check (length byte checked against a programmable maximum length)

Optionally, two status bytes (see Table 23 and Table 24) with RSSI value and CRC status can be appended in the RX FIFO.

Bit	Field Name	Description
7:0	RSSI	RSSI value

Table 23: Received Packet Status Byte 1 (first byte appended after the data)

Bit	Field Name	Description
7	CRC_OK	1: CRC for received data OK (or CRC disabled) 0: CRC error in received data
6:0	Reserved	

Table 24: Received Packet Status Byte 2 (second byte appended after the data)

Note: Register fields that control the packet handling features should only be altered when CC110L is in the IDLE state.

15.1 Packet Format

The format of the data packet can be configured and consists of the following items (see Figure 14):

- Preamble
- Synchronization word
-
- Optional length byte
- Optional address byte
- Payload
- Optional 2 byte CRC

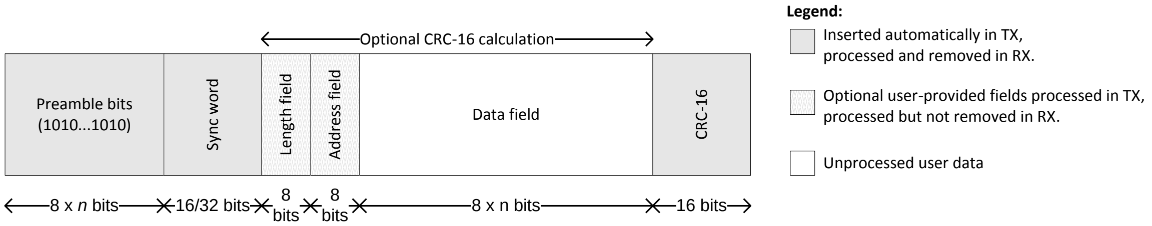


Figure 14: Packet Format

The preamble pattern is an alternating sequence of ones and zeros (10101010…). The minimum length of the preamble is programmable through the value of `MDMCFG1.NUM_PREAMBLE`. When enabling TX, the modulator will start transmitting the preamble. When the programmed number of preamble bytes has been transmitted, the modulator will send the sync word and then data from the TX FIFO if data is available. If the TX FIFO is empty, the modulator will continue to send preamble bytes until the first byte is written to the TX FIFO. The modulator will then send the sync word and then the data bytes.

The synchronization word is a two-byte value set in the `SYNC1` and `SYNC0` registers. The sync word provides byte synchronization of the incoming packet. A one-byte sync word can be emulated by setting the `SYNC1` value to the preamble pattern. It is also possible to emulate a 32 bit sync word by setting `MDMCFG2.SYNC_MODE` to 3 or 7. The sync word will then be repeated twice.

CC110L supports both constant packet length protocols and variable length protocols. Variable or fixed packet length mode can be used for packets up to 255 bytes. For longer packets, infinite packet length mode must be used.

Fixed packet length mode is selected by setting `PKTCTRL0.LENGTH_CONFIG=0`. The desired packet length is set by the `PKTLEN` register. This value must be different from 0.

In variable packet length mode, `PKTCTRL0.LENGTH_CONFIG=1`, the packet length is configured by the first byte after the sync word. The packet length is defined as the payload data, excluding the length byte and the optional CRC. The `PKTLEN` register is used to set the maximum packet length allowed in RX. Any packet received with a length byte with a value greater than `PKTLEN` will be discarded. The `PKTLEN` value must be different from 0.

With `PKTCTRL0.LENGTH_CONFIG=2`, the packet length is set to infinite and transmission and reception will continue until turned off manually. As described in the next section, this can be used to support packet formats with different length configuration than natively supported by CC110L. One should make sure that TX mode is not turned off during the transmission of the first half of any byte. Refer to the CC110L Errata Notes [3] for more details.

> **Note:** The minimum packet length supported (excluding the optional length byte and CRC) is one byte of payload data.

15.1.1 Arbitrary Length Field Configuration

The packet length register, `PKTLEN`, can be reprogrammed during receive and transmit. In combination with fixed packet length mode (`PKTCTRL0.LENGTH_CONFIG=0`), this opens the possibility to have a different length field configuration than supported for variable length packets (in variable packet length mode the length byte is the first byte after the sync word). At the start of reception, the packet length is set to a large value. The MCU reads out enough bytes to interpret the length field in the packet. Then the `PKTLEN` value is set according to this value. The end of packet will occur when the byte counter in the packet handler is equal to the `PKTLEN` register. Thus, the MCU must be able to program the correct length, before the internal counter reaches the packet length.

15.1.2 Packet Length > 255

The packet automation control register, PKTCTRL0, can be reprogrammed during TX and RX. This opens the possibility to transmit and receive packets that are longer than 256 bytes and still be able to use the packet handling hardware support. At the start of the packet, the infinite packet length mode (PKTCTRL0.LENGTH_CONFIG=2) must be active. On the TX side, the PKTLEN register is set to mod(length, 256). On the RX side the MCU reads out enough bytes to interpret the length field in the packet and sets the PKTLEN register to mod(length, 256). When less than 256 bytes remains of the packet, the MCU disables infinite packet length mode and activates fixed packet length mode (PKTCTRL0.LENGTH_CONFIG=0). When the internal byte counter reaches the PKTLEN value, the transmission or reception ends (the radio enters the state determined by TXOFF_MODE or RXOFF_MODE). Automatic CRC appending/checking can also be used (by setting PKTCTRL0.CRC_EN=1).

When for example a 600-byte packet is to be transmitted, the MCU should do the following (see also Figure 15)

- Set PKTCTRL0.LENGTH_CONFIG=2.
- Pre-program the PKTLEN register to mod(600, 256) = 88.
- Transmit at least 345 bytes (600 - 255), for example by filling the 64-byte TX FIFO six times (384 bytes transmitted).
- Set PKTCTRL0.LENGTH_CONFIG=0.
- The transmission ends when the packet counter reaches 88. A total of 600 bytes are transmitted.

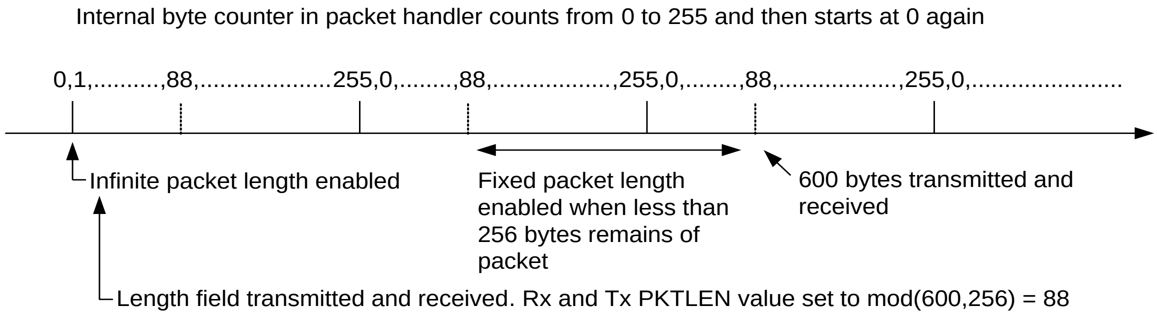


Figure 15: Packet Length > 255

15.2 Packet Filtering in Receive Mode

CC110L supports three different types of packet-filtering; address filtering, maximum length filtering, and CRC filtering.

15.2.1 Address Filtering

Setting PKTCTRL1.ADR_CHK to any other value than zero enables the packet address filter. The packet handler engine will compare the destination address byte in the packet with the programmed node address in the ADDR register and the 0x00 broadcast address when PKTCTRL1.ADR_CHK=10 or both the 0x00 and 0xFF broadcast addresses when PKTCTRL1.ADR_CHK=11. If the received address matches a valid address, the packet is received and written into the RX FIFO. If the address match fails, the packet is discarded and receive mode restarted (regardless of the MCSM1.RXOFF_MODE setting).

If the received address matches a valid address when using infinite packet length mode and address filtering is enabled, 0xFF will be written into the RX FIFO followed by the address byte and then the payload data.

15.2.2 Maximum Length Filtering

In variable packet length mode, PKTCTRL0.LENGTH_CONFIG=1, the PKTLEN.PACKET_LENGTH register value is used to set the maximum allowed packet length. If the received length byte has a larger value than this, the packet is discarded and receive mode restarted (regardless of the MCSM1.RXOFF_MODE setting).

15.2.3 CRC Filtering

The filtering of a packet when CRC check fails is enabled by setting PKTCTRL1.CRC_AUTOFLUSH=1. The CRC auto flush function will flush the entire RX FIFO if the CRC check fails. After auto flushing the RX FIFO, the next state depends on the MCSM1.RXOFF_MODE setting.

When using the auto flush function, the maximum packet length is 63 bytes in variable packet length mode and 64 bytes in fixed packet length mode. Note that when PKTCTRL1.APPEND_STATUS is enabled, the maximum allowed packet length is reduced by two bytes in order to make room in the RX FIFO for the two status bytes appended at the end of the packet. Since the entire RX FIFO is flushed when the CRC check fails, the previously received packet must be read out of the FIFO before receiving the current packet. The MCU must not read from the current packet until the CRC has been checked as OK.

15.3 Packet Handling in Transmit Mode

The payload that is to be transmitted must be written into the TX FIFO. The first byte written must be the length byte when variable packet length is enabled. The length byte has a value equal to the payload of the packet (including the optional address byte). If address recognition is enabled on the receiver, the second byte written to the TX FIFO must be the address byte.

If fixed packet length is enabled, the first byte written to the TX FIFO should be the address (assuming the receiver uses address recognition).

The modulator will first send the programmed number of preamble bytes. If data is available in the TX FIFO, the modulator will send the two-byte (optionally 4-byte) sync word followed by the payload in the TX FIFO. If CRC is enabled, the checksum is calculated over all the data pulled from the TX FIFO, and the result is sent as two extra bytes following the payload data. If the TX FIFO runs empty before the complete packet has been transmitted, the radio will enter TXFIFO_UNDERFLOW state. The only way to exit this state is by issuing an SFTX strobe. Writing to the TX FIFO after it has underflowed will not restart TX mode.

15.4 Packet Handling in Receive Mode

In receive mode, the demodulator and packet handler will search for a valid preamble and the sync word. When found, the demodulator has obtained both bit and byte synchronization and will receive the first payload byte.

When variable packet length mode is enabled, the first byte is the length byte. The packet handler stores this value as the packet length and receives the number of bytes indicated by the length byte. If fixed packet length mode is used, the packet handler will accept the programmed number of bytes.

Next, the packet handler optionally checks the address and only continues the reception if the address matches. If automatic CRC check is enabled, the packet handler computes CRC and matches it with the appended CRC checksum.

At the end of the payload, the packet handler will optionally write two extra packet status bytes (see Table 23 and Table 24) that contain CRC status, link quality indication, and RSSI value.

15.5 Packet Handling in Firmware

When implementing a packet oriented radio protocol in firmware, the MCU needs to know when a packet has been received/transmitted. Additionally, for packets longer than 64 bytes, the RX FIFO needs to be read while in RX and the TX FIFO needs to be refilled while in TX. This means that the MCU needs to know the number of bytes that can be read from or written to the RX FIFO and TX FIFO respectively. There are two possible solutions to get the necessary status information:

a) Interrupt Driven Solution

The GDO pins can be used in both RX and TX to give an interrupt when a sync word has been received/transmitted or when a complete packet has been received/transmitted by setting IOCFGx.GDOx_CFG=0x06. In addition, there are two configurations for the IOCFGx.GDOx_CFG register that can be used as an interrupt source to provide information on how many bytes that are in the RX FIFO and TX FIFO respectively. The

IOCFGx.GDOx_CFG=0x00 and the IOCFGx.GDOx_CFG=0x01 configurations are associated with the RX FIFO while the IOCFGx.GDOx_CFG=0x02 and the IOCFGx.GDOx_CFG=0x03 configurations are associated with the TX FIFO. See Table 36 for more information.

b) SPI Polling

The PKTSTATUS register can be polled at a given rate to get information about the current GDO2 and GDO0 values respectively. The RXBYTES and TXBYTES registers can be polled at a given rate to get information about the number of bytes in the RX FIFO and TX FIFO respectively. Alternatively, the number of bytes in the RX FIFO and TX FIFO can be read from the chip status byte returned on the MISO line each time a header byte, data byte, or command strobe is sent on the SPI bus.

It is recommended to employ an interrupt driven solution since high rate SPI polling reduces the RX sensitivity. Furthermore, as explained in Section 10.3 and the CC110L Errata Notes [3], when using SPI polling, there is a small, but finite, probability that a single read from registers PKTSTATUS , RXBYTES and TXBYTES is being corrupt. The same is the case when reading the chip status byte.

16 Modulation Formats

CC110L supports amplitude, frequency, and phase shift modulation formats. The desired modulation format is set in the MDMCFG2.MOD_FORMAT register.

Optionally, the data stream can be Manchester coded by the modulator and decoded by the demodulator. This option is enabled by setting MDMCFG2.MANCHESTER_EN=1.

Note: Manchester encoding is not supported at the same time as using 4-FSK modulation.

16.1 Frequency Shift Keying

CC110L supports 2-(G)FSK and 4-FSK modulation. When selecting 4-FSK, the preamble and sync word to be received needs to be 2-FSK (see Figure 16).

When 2-FSK/GFSK/4-FSK modulation is used, the DEVIATN register specifies the expected frequency deviation of incoming signals in RX and should be the same as the deviation of the transmitted signal for demodulation to be performed reliably and robustly.

The frequency deviation is programmed with the DEVIATION_M and DEVIATION_E values in the DEVIATN register. The value has an exponent/mantissa form, and the resultant deviation is given by:

$$f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$$

The symbol encoding is shown in Table 25.

Format	Symbol	Coding
2-FSK/GFSK	‘0’	– Deviation
	‘1’	+ Deviation
4-FSK	‘01’	– Deviation
	‘00’	– 1/3·Deviation
	‘10’	+1/3·Deviation
	‘11’	+ Deviation

Table 25: Symbol Encoding for 2-FSK/GFSK and 4-FSK Modulation

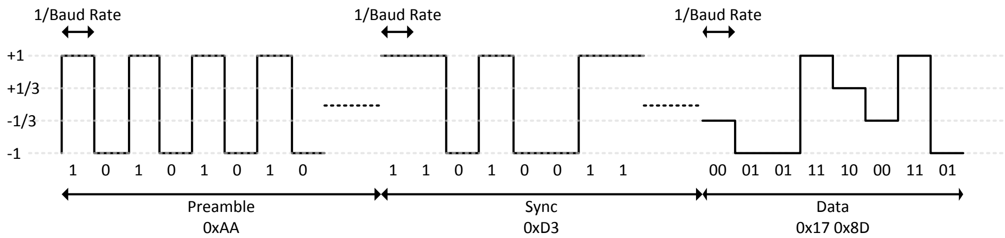


Figure 16: Data Sent Over the Air (MDMCFG2.MOD_FORMAT=100)

16.2 Amplitude Modulation

The amplitude modulation supported by CC110L is On-Off Keying (OOK).

OOK modulation simply turns the PA on or off to modulate ones and zeros respectively.

When using OOK, the AGC settings from the SmartRF Studio [4] preferred FSK settings are not optimum. DN022 [11] gives guidelines on how to find optimum OOK settings from the preferred settings in SmartRF Studio [4]. The **DEVIATN** register setting has no effect in either TX or RX when using OOK.

17 Received Signal Qualifiers and RSSI

CC110L has several qualifiers that can be used to increase the likelihood that a valid sync word is detected:

- Sync Word Qualifier
- RSSI
- Carrier Sense
- Clear Channel Assessment

17.1 Sync Word Qualifier

If sync word detection in RX is enabled in the MDMCFG2 register, the CC110L will not start filling the RX FIFO and perform the packet filtering described in Section 15.2 before a valid sync word has been detected. The sync word qualifier mode is set by MDMCFG2.SYNC_MODE and is summarized in Table 26. Carrier sense in Table 26 is described in Section 17.3.

MDMCFG2. SYNC_MODE	Sync Word Qualifier Mode
000	No preamble/sync
001	15/16 sync word bits detected
010	16/16 sync word bits detected
011	30/32 sync word bits detected
100	No preamble/sync + carrier sense above threshold
101	15/16 + carrier sense above threshold
110	16/16 + carrier sense above threshold
111	30/32 + carrier sense above threshold

Table 26: Sync Word Qualifier Mode

17.2 RSSI

The RSSI value is an estimate of the signal power level in the chosen channel. This value is based on the current gain setting in the RX chain and the measured signal level in the channel.

In RX mode, the RSSI value can be read continuously from the RSSI status register until the demodulator detects a sync word (when sync word detection is enabled). At that point the RSSI readout value is frozen until the next time the chip enters the RX state.

> **Note**: It takes some time from the radio enters RX mode until a valid RSSI value is present in the RSSI register. Please see DN505 [9] for details on how the RSSI response time can be estimated.

The RSSI value is given in dBm with a ½ dB resolution. The RSSI update rate, f_{RSSI}, depends on the receiver filter bandwidth ($BW_{channel}$ is defined in Section 13) and AGCCTRL0.FILTER_LENGTH.

$$f_{RSSI} = \frac{2 \cdot BW_{channel}}{8 \cdot 2^{FILTER\_LENGTH}}$$

If PKTCTRL1.APPEND_STATUS is enabled, the last RSSI value of the packet is automatically added to the first byte appended after the payload.

The RSSI value read from the RSSI status register is a 2's complement number. The following procedure can be used to convert the RSSI reading to an absolute power level (RSSI_dBm)

1) Read the RSSI status register

2) Convert the reading from a hexadecimal number to a decimal number (RSSI_dec)

3) If RSSI_dec ≥ 128 then RSSI_dBm = (RSSI_dec - 256)/2 – RSSI_offset

4) Else if RSSI_dec < 128 then RSSI_dBm = (RSSI_dec)/2 – RSSI_offset

Table 27 gives typical values for the RSSI_offset. Figure 17 and Figure 18 show typical plots of RSSI readings as a function of input power level for different data rates.

Data rate [kBaud]	RSSI_offset [dB], 433 MHz	RSSI_offset [dB], 868 MHz
1.2	74	74
38.4	74	74
250	74	74

Table 27: Typical RSSI_offset Values

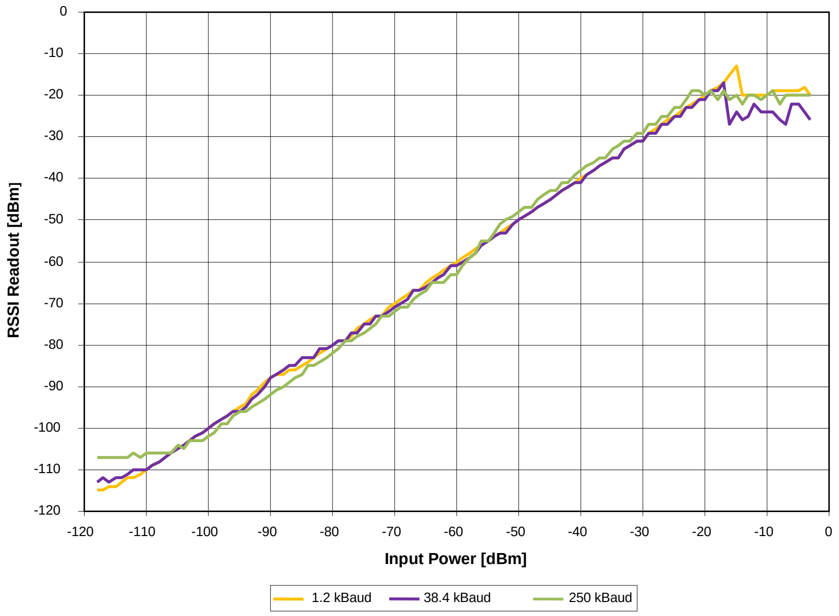


Figure 17: Typical RSSI Value vs. Input Power Level for Different Data Rates at 433 MHz

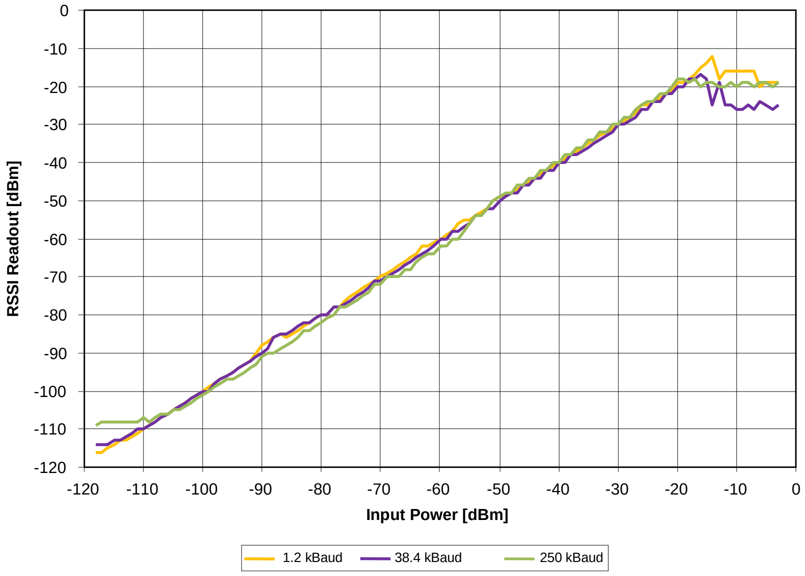


Figure 18: Typical RSSI Value vs. Input Power Level for Different Data Rates at 868 MHz

17.3 Carrier Sense (CS)

Carrier sense (CS) is used as a sync word qualifier and for Clear Channel Assessment (see Section 17.4). CS can be asserted based on two conditions which can be individually adjusted:

- CS is asserted when the RSSI is above a programmable absolute threshold, and de-asserted when RSSI is below the same threshold (with hysteresis). See more in Section 17.3.1.
- CS is asserted when the RSSI has increased with a programmable number of dB from one RSSI sample to the next, and de-asserted when RSSI has decreased with the same number of dB. This setting is not dependent on the absolute signal level and is thus useful to detect signals in environments with time varying noise floor. See more in Section 17.3.2.

Carrier sense can be used as a sync word qualifier that requires the signal level to be higher than the threshold for a sync word search to be performed and is set by setting MDMCFG2. The carrier sense signal can be observed on one of the GDO pins by setting IOCFGx.GDOx_CFG=14 and in the status register bit PKTSTATUS.CS.

Other uses of Carrier sense include the TX-if-CCA function (see Section 17.4 on page 38) and the optional fast RX termination (see Section 18.5 on page 41).

CS can be used to avoid interference from other RF sources in the ISM bands.

17.3.1 CS Absolute Threshold

The absolute threshold related to the RSSI value depends on the following register fields:

- AGCCTRL2.MAX_LNA_GAIN
- AGCCTRL2.MAX_DVGA_GAIN
- AGCCTRL1.CARRIER_SENSE_ABS_THR
- AGCCTRL2.MAGN_TARGET

For given AGCCTRL2.MAX_LNA_GAIN and AGCCTRL2.MAX_DVGA_GAIN settings, the absolute threshold can be adjusted ±7 dB in steps of 1 dB using CARRIER_SENSE_ABS_THR.

The MAGN_TARGET setting is a compromise between blocker tolerance/selectivity and sensitivity. The value sets the desired signal level in the channel into the demodulator. Increasing this value reduces the headroom for blockers, and therefore close-in selectivity. It is strongly recommended to use SmartRF Studio [4] to generate the correct MAGN_TARGET setting. Table 28 shows the typical RSSI readout values at the CS threshold at 250 kBaud data rate. The default reset value for CARRIER_SENSE_ABS_THR (0 dB) has been used. MAGN_TARGET=111 (42 dB) have been used for the 250 kBaud data rate. For other data rates, the user must generate similar tables to find the CS absolute threshold.

		MAX_DVGA_GAIN[1:0]			
		00	01	10	11
MAX_LNA_GAIN[2:0]	000	−90.5	−84.5	−78.5	−72.5
	001	−88	−82	−76	−70
	010	−84.5	−78.5	−72	−66
	011	−82.5	−76.5	−70	−64
	100	−80.5	−74.5	−68	−62
	101	−78	−72	−66	−60
	110	−76.5	−70	−64	−58
	111	−74.5	−68	−62	−56

Table 28: Typical RSSI Value in dBm at CS Threshold with MAGN_TARGET = 7 (42 dB) at 250 kBaud, 868 MHz

If the threshold is set high, i.e. only strong signals are wanted, the threshold should be adjusted upwards by first reducing the MAX_LNA_GAIN value and then the MAX_DVGA_GAIN value. This will reduce power consumption in the receiver front end, since the highest gain settings are avoided.

17.3.2 CS Relative Threshold

The relative threshold detects sudden changes in the measured signal level. This setting does not depend on the absolute signal level and is thus useful to detect signals in environments with a time varying noise floor. The register field AGCCTRL1.CARRIER_SENSE_REL_THR is used to enable/disable relative CS, and to select threshold of 6 dB, 10 dB, or 14 dB RSSI change.

17.4 Clear Channel Assessment (CCA)

The Clear Channel Assessment (CCA) is used to indicate if the current channel is free or busy. The current CCA state is viewable on any of the GDO pins by setting IOCFGx.GDOx_CFG=0x09.

MCSM1.CCA_MODE selects the mode to use when determining CCA.

When the STX or SFSTXON command strobe is given while CC110L is in the RX state, the TX or FSTXON state is only entered if the clear channel requirements are fulfilled. Otherwise, the chip will remain in RX. If the channel then becomes available, the radio will not enter TX or FSTXON state before a new strobe command is sent on the SPI interface. This feature is called TX-if-CCA. Four CCA requirements can be programmed:

- Always (CCA disabled, always goes to TX)
- If RSSI is below threshold
- Unless currently receiving a packet
- Both the above (RSSI below threshold and not currently receiving a packet)

18 Radio Control

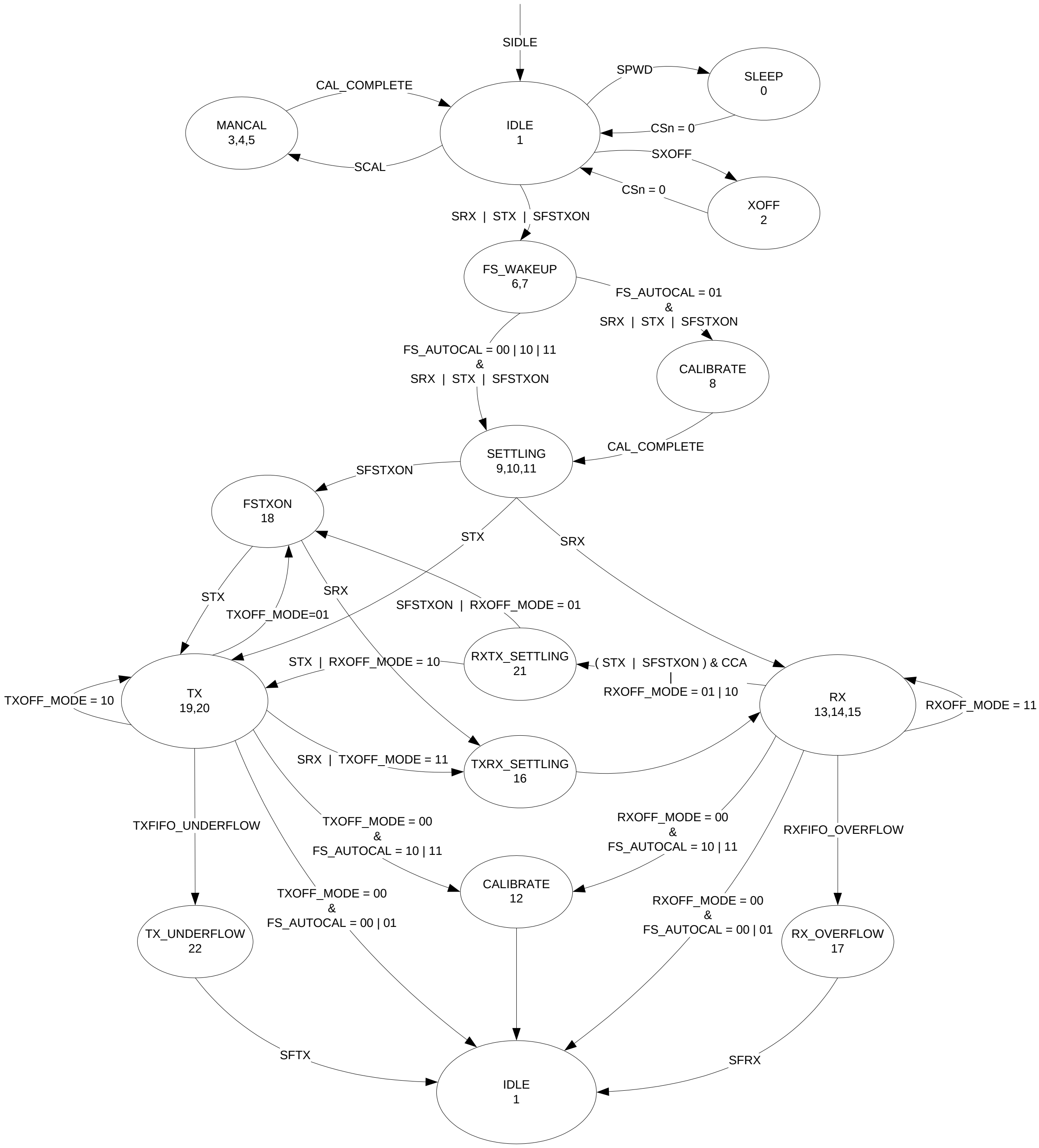


Figure 19: Complete Radio Control State Diagram

CC110L has a built-in state machine that is used to switch between different operational states (modes). The change of state is done either by using command strobes or by internal events such as TX FIFO underflow.

A simplified state diagram, together with typical usage and current consumption, is shown in Figure 10 on page 22. The complete radio control state diagram is shown in Figure 19. The numbers refer to the state number readable in the `MARCSTATE` status register. This register is primarily for test purposes.

18.1 Power-On Start-Up Sequence

When the power supply is turned on, the system must be reset. This is achieved by one of the two sequences described below, i.e. automatic power-on reset (POR) or manual reset. After the automatic power-on reset or manual reset, it is also recommended to change the signal that is output on the GDO0 pin. The default setting is to output a clock signal with a frequency of CLK_XOSC/192. However, to optimize performance in TX and RX, an alternative GDO setting from the settings found in Table 36 on page 49 should be selected.

18.1.1 Automatic POR

A power-on reset circuit is included in the CC110L. The minimum requirements stated in Table 16 must be followed for the power-on reset to function properly. The internal power-up sequence is completed when `CHIP_RDYn` goes low. `CHIP_RDYn` is observed on the SO pin after CSn is pulled low. See Section 10.1 for more details on `CHIP_RDYn`.

When the CC110L reset is completed, the chip will be in the IDLE state and the crystal oscillator will be running. If the chip has had sufficient time for the crystal oscillator to stabilize after the power-on-reset, the SO pin will go low immediately after taking CSn low. If CSn is taken low before reset is completed, the SO pin will first go high, indicating that the crystal oscillator is not stabilized, before going low as shown in Figure 20.

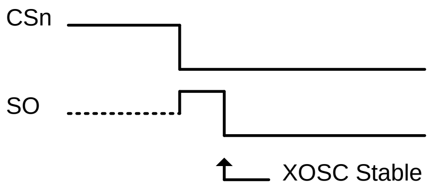


Figure 20: Power-On Reset

18.1.2 Manual Reset

The other global reset possibility on CC110L uses the `SRES` command strobe. By issuing this strobe, all internal registers and states are set to the default, IDLE state. The manual power-up sequence is as follows (see Figure 21):

- Set SCLK = 1 and SI = 0.
- Strobe CSn low / high.
- Hold CSn low and then high for at least 40 µs relative to pulling CSn low
- Pull CSn low and wait for SO to go low (`CHIP_RDYn`).
- Issue the `SRES` strobe on the SI line.
- When SO goes low again, reset is complete and the chip is in the IDLE state.

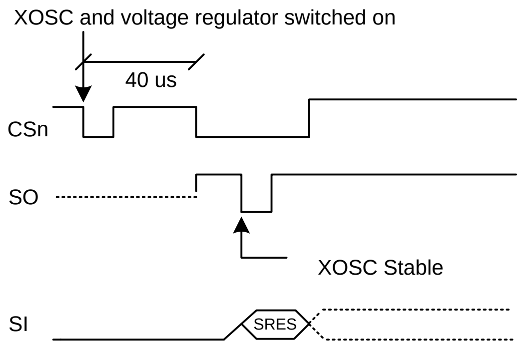


Figure 21: Power-On Reset with `SRES`

Note that the above reset procedure is only required just after the power supply is first turned on. If the user wants to reset the CC110L after this, it is only necessary to issue an `SRES` command strobe.

18.2 Crystal Control

The crystal oscillator (XOSC) is either automatically controlled or always on, if `MCSM0.XOSC_FORCE_ON` is set.

In the automatic mode, the XOSC will be turned off if the `SXOFF` or `SPWD` command strobes are issued; the state machine then goes to XOFF or SLEEP respectively. This can only be done from the IDLE state. The XOSC will be turned off when CSn is released (goes high). The XOSC will be automatically turned on again when CSn goes low. The state machine will then go to the IDLE state. The SO pin on the SPI interface must be pulled low before the SPI interface is ready to be used as described in Section 10.1 on page 25.

If the XOSC is forced on, the crystal will always stay on even in the SLEEP state.

Crystal oscillator start-up time depends on crystal ESR and load capacitances. The electrical specification for the crystal oscillator can be found in Section 4.4 on page 14.

18.3 Voltage Regulator Control

The voltage regulator to the digital core is controlled by the radio controller. When the chip enters the SLEEP state which is the state with the lowest current consumption, the voltage regulator is disabled. This occurs after CSn is released when a `SPWD` command strobe has been sent on the SPI interface. The chip is then in the SLEEP state. Setting CSn low again will turn on the regulator and crystal oscillator and make the chip enter the IDLE state.

18.4 Active Modes (RX and TX)

CC110L has two active modes: receive and transmit. These modes are activated directly by the MCU by using the `SRX` and `STX` command strobes.

The frequency synthesizer must be calibrated regularly. **CC110L** has one manual calibration option (using the `SCAL` strobe), and three automatic calibration options that are controlled by the `MCSM0.FS_AUTOCAL` setting:

- Calibrate when going from IDLE to either RX or TX (or FSTXON)
- Calibrate when going from either RX or TX to IDLE automatically[1]
- Calibrate every fourth time when going from either RX or TX to IDLE automatically[1]

If the radio goes from TX or RX to IDLE by issuing an `SIDLE` strobe, calibration will not be performed. The calibration takes a constant number of XOSC cycles; see Table 29 for timing details regarding calibration.

When RX is activated, the chip will remain in receive mode until a packet is successfully received or until RX mode terminated due to lack of carrier sense (see Section 18.5). The probability that a false sync word is detected can be reduced by using CS together with maximum sync word length as described in Section 17. After a packet is successfully received, the radio controller goes to the state indicated by the `MCSM1.RXOFF_MODE` setting. The possible destinations are:

- IDLE
- FSTXON: Frequency synthesizer on and ready at the TX frequency. Activate TX with `STX`
- TX: Start sending preamble
- RX: Start search for a new packet

> **Note:** When `MCSM1.RXOFF_MODE=11` and a packet has been received, it will take some time before a valid RSSI value is present in the `RSSI` register again even if the radio has never exited RX mode. This time is the same as the RSSI response time discussed in DN505 [8].

Similarly, when TX is active the chip will remain in the TX state until the current packet has been successfully transmitted. Then the state will change as indicated by the `MCSM1.TXOFF_MODE` setting. The possible destinations are the same as for RX.

The MCU can manually change the state from RX to TX and vice versa by using the command strobes. If the radio controller is currently in transmit and the `SRX` strobe is used, the current transmission will be ended and the transition to RX will be done.

If the radio controller is in RX when the `STX` or `SFSTXON` command strobes are used, the TX-if-CCA function will be used. If the channel is not clear, the chip will remain in RX. The `MCSM1.CCA_MODE` setting controls the conditions for clear channel assessment. See Section 17.4 on page 38 for details.

The `SIDLE` command strobe can always be used to force the radio controller to go to the IDLE state.

18.5 RX Termination

If the system expects the transmission to have started when entering RX mode, the `MCSM2.RX_TIME_RSSI` function can be used. The radio controller will then terminate RX if the first valid carrier sense sample indicates no carrier (RSSI below threshold). See Section 17.3 on page 37 for details on Carrier Sense.

For OOK modulation, lack of carrier sense is only considered valid after eight symbol

[1] Not forced in IDLE by issuing an SIDLE strobe

periods. Thus, the MCSM2.RX_TIME_RSSI function can be used in OOK mode when the distance between two "1" symbols is eight or less.

18.6 Timing

18.6.1 Overall State Transition Times

The main radio controller needs to wait in certain states in order to make sure that the internal analog/digital parts have settled down and are ready to operate in the new states. A number of factors are important for the state transition times:

- The crystal oscillator frequency, f_{xosc}
- OOK used or not
- The data rate in cases where OOK is used
- The value of the TEST0, TEST1, and FSCAL3 registers

Table 29 shows timing in crystal clock cycles for key state transitions.

Note that the TX to IDLE transition time is a function of data rate ($f_{baudrate}$). When OOK is used (i.e. FREND0.PA_POWER=001_b), TX to IDLE will require $1/8 \cdot f_{baudrate}$ longer times than the time stated in Table 29.

Description	Transition Time (FREND0.PA_POWER=0)	Transition Time [µs]
IDLE to RX, no calibration	$1953/f_{xosc}$	75.1
IDLE to RX, with calibration	$1953/f_{xosc}$ + FS calibration Time	799
IDLE to TX/FSTXON, no calibration	$1954/f_{xosc}$	75.2
IDLE to TX/FSTXON, with calibration	$1953/f_{xosc}$ + FS calibration Time	799
TX to RX switch	$782/f_{xosc} + 0.25/f_{baudrate}$	31.1
RX to TX switch	$782/f_{xosc}$	30.1
TX to IDLE, no calibration	$\sim 0.25/f_{baudrate}$	~1
TX to IDLE, with calibration	$\sim 0.25/f_{baudrate}$ + FS calibration Time	725
RX to IDLE, no calibration	$2/f_{xosc}$	~0.1
RX to IDLE, with calibration	$2/f_{xosc}$ + FS calibration Time	724
Manual calibration	$283/f_{xosc}$ + FS calibration Time	735

Table 29: Overall State Transition Times (Example for 26 MHz crystal oscillator, 250 kBaud data rate, and TEST0 = 0x0B (maximum calibration time)).

18.6.2 Frequency Synthesizer Calibration Time

Table 30 summarizes the frequency synthesizer (FS) calibration times for possible settings of TEST0 and FSCAL3.CHP_CURR_CAL_EN. Setting FSCAL3.CHP_CURR_CAL_EN to 00_b disables the charge pump calibration stage. TEST0 is set to the values recommended by SmartRF Studio software [4]. The possible values for TEST0 when operating with different frequency bands are 0x09 and 0x0B. SmartRF Studio software [4] always sets FSCAL3.CHP_CURR_CAL_EN to 10_b.

The calibration time can be reduced from 712/724 µs to 145/157 µs. See Section 26.2 on page 50 for more details.

TEST0	FSCAL3.CHP_CURR_CAL_EN	FS Calibration Time f_{xosc} = 26 MHz	FS Calibration Time f_{xosc} = 27 MHz
0x09	00_b	$3764/f_{xosc}$ = 145 us	$3764/f_{xosc}$ = 139 us
0x09	10_b	$18506/f_{xosc}$ = 712 us	$18506/f_{xosc}$ = 685 us
0x0B	00_b	$4073/f_{xosc}$ = 157 us	$4073/f_{xosc}$ = 151 us
0x0B	10_b	$18815/f_{xosc}$ = 724 us	$18815/f_{xosc}$ = 697 us

Table 30. Frequency Synthesizer Calibration Times (26/27 MHz crystal)

19 Data FIFO

The CC110L contains two 64-byte FIFOs, one for received data and one for data to be transmitted. The SPI interface is used to read from the RX FIFO and write to the TX FIFO. Section 10.5 contains details on the SPI FIFO access. The FIFO controller will detect overflow in the RX FIFO and underflow in the TX FIFO.

When writing to the TX FIFO it is the responsibility of the MCU to avoid TX FIFO overflow. A TX FIFO overflow will result in an error in the TX FIFO content.

Likewise, when reading the RX FIFO the MCU must avoid reading the RX FIFO past its empty value since a RX FIFO underflow will result in an error in the data read out of the RX FIFO.

The chip status byte that is available on the SO pin while transferring the SPI header and contains the fill grade of the RX FIFO if the access is a read operation and the fill grade of the TX FIFO if the access is a write operation. Section 10.1 on page 25 contains more details on this.

The number of bytes in the RX FIFO and TX FIFO can be read from the status registers `RXBYTES.NUM_RXBYTES` and `TXBYTES.NUM_TXBYTES` respectively. If a received data byte is written to the RX FIFO at the exact same time as the last byte in the RX FIFO is read over the SPI interface, the RX FIFO pointer is not properly updated and the last read byte will be duplicated. To avoid this problem, the RX FIFO should never be emptied before the last byte of the packet is received.

For packet lengths less than 64 bytes it is recommended to wait until the complete packet has been received before reading it out of the RX FIFO.

If the packet length is larger than 64 bytes, the MCU must determine how many bytes can be read from the RX FIFO (`RXBYTES.NUM_RXBYTES`-1). The following software routine can be used:

1. Read `RXBYTES.NUM_RXBYTES` repeatedly at a rate specified to be at least twice that of which RF bytes are received until the same value is returned twice; store value in *n*.
2. If *n* < # of bytes remaining in packet, read *n*-1 bytes from the RX FIFO.
3. Repeat steps 1 and 2 until *n* = # of bytes remaining in packet.
4. Read the remaining bytes from the RX FIFO.

The 4-bit `FIFOTHR.FIFO_THR` setting is used to program threshold points in the FIFOs.

Table 31 lists the 16 `FIFO_THR` settings and the corresponding thresholds for the RX and TX FIFOs. The threshold value is coded in opposite directions for the RX FIFO and TX FIFO. This gives equal margin to the overflow and underflow conditions when the threshold is reached.

FIFO_THR	Bytes in TX FIFO	Bytes in RX FIFO
0 (0000)	61	4
1 (0001)	57	8
2 (0010)	53	12
3 (0011)	49	16
4 (0100)	45	20
5 (0101)	41	24
6 (0110)	37	28
7 (0111)	33	32
8 (1000)	29	36
9 (1001)	25	40
10 (1010)	21	44
11 (1011)	17	48
12 (1100)	13	52
13 (1101)	9	56
14 (1110)	5	60
15 (1111)	1	64

Table 31: FIFO_THR Settings and the Corresponding FIFO Thresholds

A signal will assert when the number of bytes in the FIFO is equal to or higher than the programmed threshold. This signal can be viewed on the GDO pins (see Table 36 on page 49).

Figure 22 shows the number of bytes in both the RX FIFO and TX FIFO when the threshold signal toggles in the case of `FIFO_THR=13`. Figure 23 shows the signal on the GDO pin as the respective FIFO is filled above the threshold, and then drained below in the case of `FIFO_THR=13`.

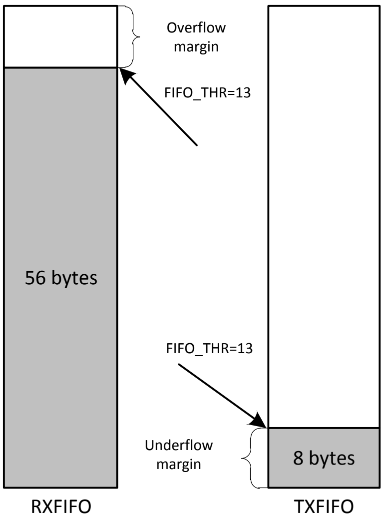


Figure 22 Example of FIFOs at Threshold

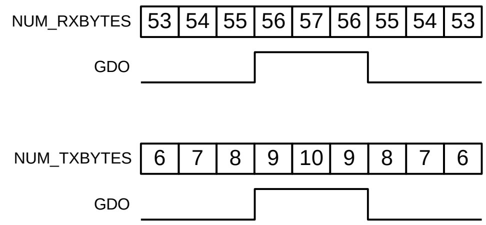


Figure 23: Number of Bytes in FIFO vs. the GDO Signal (`GDOx_CFG=0x00` in RX and `GDOx_CFG=0x02` in TX, `FIFO_THR=13`)

20 Frequency Programming

The frequency programming in **CC110L** is designed to minimize the programming needed when changing frequency.

To set up a system with channel numbers, the desired channel spacing is programmed with the `MDMCFG0.CHANSPC_M` and `MDMCFG1.CHANSPC_E` registers. The channel spacing registers are mantissa and exponent respectively. The base or start frequency is set by the 24 bit frequency word located in the `FREQ2`, `FREQ1`, and `FREQ0` registers. This word will typically be set to the centre of the lowest channel frequency that is to be used.

The desired channel number is programmed with the 8-bit channel number register, `CHANNR.CHAN`, which is multiplied by the channel offset. The resultant carrier frequency is given by:

$$f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot (FREQ + CHAN \cdot ((256 + CHANSPC\_M) \cdot 2^{CHANSPC\_E-2}))$$

With a 26 MHz crystal the maximum channel spacing is 405 kHz. To get e.g. 1 MHz channel spacing, one solution is to use 333 kHz channel spacing and select each third channel in `CHANNR.CHAN`.

The preferred IF frequency is programmed with the `FSCTRL1.FREQ_IF` register. The IF frequency is given by:

$$f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$$

If any frequency programming register is altered when the frequency synthesizer is running, the synthesizer may give an undesired response. Hence, the frequency should only be updated when the radio is in the IDLE state

21 VCO

The VCO is completely integrated on-chip.

21.1 VCO and PLL Self-Calibration

The VCO characteristics vary with temperature and supply voltage changes as well as the desired operating frequency. In order to ensure reliable operation, **CC110L** includes frequency synthesizer self-calibration circuitry. This calibration should be done regularly, and must be performed after turning on power and before using a new frequency (or channel). The number of XOSC cycles for completing the PLL calibration is given in Table 29 on page 42.

The calibration can be initiated automatically or manually. The synthesizer can be automatically calibrated each time the synthesizer is turned on, or each time the synthesizer is turned off automatically. This is configured with the `MCSM0.FS_AUTOCAL` register setting. In manual mode, the calibration is initiated when the SCAL command strobe is activated in the IDLE mode.

Note: The calibration values are maintained in SLEEP mode, so the calibration is still valid after waking up from SLEEP mode unless supply voltage or temperature has changed significantly.

To check that the PLL is in lock, the user can program register IOCFGx.GDOx_CFG to 0x0A, and use the lock detector output available on the GDOx pin as an interrupt for the MCU (x = 0,1, or 2). A positive transition on the GDOx pin means that the PLL is in lock. As an alternative the user can read register FSCAL1. The PLL is in lock if the register content is different from 0x3F. Refer also to the CC110L Errata Notes [3].

For more robust operation, the source code could include a check so that the PLL is re-calibrated until PLL lock is achieved if the PLL does not lock the first time.

22 Voltage Regulators

CC110L contains several on-chip linear voltage regulators that generate the supply voltages needed by low-voltage modules. These voltage regulators are invisible to the user, and can be viewed as integral parts of the various modules. The user must however make sure that the absolute maximum ratings and required pin voltages in Table 19 and Table 17 are not exceeded.

By setting the CSn pin low, the voltage regulator to the digital core turns on and the crystal oscillator starts. The SO pin on the SPI interface must go low before the first positive edge of SCLK (setup time is given in Table 19).

If the chip is programmed to enter power-down mode (SPWD strobe issued), the power will be turned off after CSn goes high. The power and crystal oscillator will be turned on again when CSn goes low.

The voltage regulator for the digital core requires one external decoupling capacitor.

The voltage regulator output should only be used for driving the CC110L.

23 Output Power Programming

The RF output power level from the device has two levels of programmability. The PATABLE register can hold two user selected output power settings and the FREND0.PA_POWER value selects the PATABLE entry to use (0 or 1). PATABLE must be programmed in burst mode if writing to other entries than PATABLE[0].See Section 10.6 on page 27 for more programming details.

For OOK modulation, FREND0.PA_POWER should be 1 and the logic 0 and logic 1 power levels shall be programmed to index 0 and 1 respectively. For all other modulation formats, the desired output power should be programmed to index 0.

Table 34 contains recommended PATABLE settings for various output levels and frequency bands. DN013 [10] gives the complete tables for the different frequency bands using multi-layer inductors. Using PA settings from 0x61 to 0x6F is not allowed. Table 35 contains output power and current consumption for default PATABLE setting (0xC6). The measurements are done on [2].

Note: All content of the PATABLE except for the first byte (index 0) is lost when entering the SLEEP state.

	868 MHz		915 MHz	
Output Power [dBm]	**Setting**	**Current Consumption, Typ. [mA]**	**Setting**	**Current Consumption, Typ. [mA]**
12/11	0xC0	34.2	0xC0	33.4
10	0xC5	30.0	0xC3	30.7
7	0xCD	25.8	0xCC	25.7
5	0x86	19.9	0x84	20.2
0	0x50	16.8	0x8E	17.2
−6	0x37	16.4	0x38	17.0
−10	0x26	14.5	0x27	14.8
−15	0x1D	13.3	0x1E	13.3
−20	0x17	12.6	0x0E	12.5
−30	0x03	12.0	0x03	11.9

Table 32: Optimum PATABLE Settings for Various Output Power Levels Using Wire-Wound Inductors in 868/915 MHz Frequency Bands

	868 MHz		915 MHz	
Default Power Setting	**Output Power [dBm]**	**Current Consumption, Typ. [mA]**	**Output Power [dBm]**	**Current Consumption, Typ. [mA]**
0xC6	9.6	29.4	8.9	28.7

Table 33: Output Power and Current Consumption for Default PATABLE Setting Using Wire-Wound Inductors in 868/915 MHz Frequency Bands

	868 MHz		915 MHz	
Output Power [dBm]	**Setting**	**Current Consumption, Typ. [mA]**	**Setting**	**Current Consumption, Typ. [mA]**
10	0xC2	32.4	0xC0	31.8
7	0xCB	26.8	0xC7	26.9
5	0x81	21.0	0xCD	24.3
0	0x50	16.9	0x8E	16.7
−10	0x27	15.0	0x27	14.9
−15	0x1E	13.4	0x1E	13.4
−20	0x0F	12.7	0x0E	12.6
−30	0x03	12.1	0x03	12.0

Table 34: Optimum PATABLE Settings for Various Output Power Levels Using Multi-layer Inductors in 868/915 MHz Frequency Bands

	868 MHz		915 MHz	
Default Power Setting	**Output Power [dBm]**	**Current Consumption, Typ. [mA]**	**Output Power [dBm]**	**Current Consumption, Typ. [mA]**
0xC6	8.5	29.5	7.2	27.4

Table 35: Output Power and Current Consumption for Default PATABLE Setting Using Multi-layer Inductors in 868/915 MHz Frequency Bands

24 General Purpose / Test Output Control Pins

The three digital output pins GDO0, GDO1, and GDO2 are general control pins configured with IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG, and IOCFG2.GDO2_CFG respectively. Table 36 shows the different signals that can be monitored on the GDO pins. These signals can be used as inputs to the MCU.

GDO1 is the same pin as the SO pin on the SPI interface, thus the output programmed on this pin will only be valid when CSn is high. The default value for GDO1 is 3-stated which is useful when the SPI interface is shared with other devices.

The default value for GDO0 is a 135-141 kHz clock output (XOSC frequency divided by 192). Since the XOSC is turned on at power-on-reset, this can be used to clock the MCU in systems with only one crystal. When the MCU is up and running, it can change the clock frequency by writing to IOCFG0.GDO0_CFG.

If the IOCFGx.GDOx_CFG setting is less than 0x20 and IOCFGx_GDOx_INV is 0 (1), the GDO0 and GDO2 pins will be hardwired to 0 (1), and the GDO1 pin will be hardwired to 1 (0) in the SLEEP state. These signals will be hardwired until the CHIP_RDYn signal goes low.

If the IOCFGx.GDOx_CFG setting is 0x20 or higher, the GDO pins will work as programmed also in SLEEP state. As an example, GDO1 is high impedance in all states if IOCFG1.GDO1_CFG=0x2E.

GDOx_CFG[5:0]	Description
0 (0x00)	Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold. De-asserts when RX FIFO is drained below the same threshold.
1 (0x01)	Associated to the RX FIFO: Asserts when RX FIFO is filled at or above the RX FIFO threshold or the end of packet is reached. De-asserts when the RX FIFO is empty.
2 (0x02)	Associated to the TX FIFO: Asserts when the TX FIFO is filled at or above the TX FIFO threshold. De-asserts when the TX FIFO is below the same threshold.
3 (0x03)	Associated to the TX FIFO: Asserts when TX FIFO is full. De-asserts when the TX FIFO is drained below the TX FIFO threshold.
4 (0x04)	Asserts when the RX FIFO has overflowed. De-asserts when the FIFO has been flushed.
5 (0x05)	Asserts when the TX FIFO has underflowed. De-asserts when the FIFO is flushed.
6 (0x06)	Asserts when sync word has been sent / received, and de-asserts at the end of the packet. In RX, the pin will also de-assert when a packet is discarded due to address or maximum length filtering or when the radio enters RXFIFO_OVERFLOW state. In TX the pin will de-assert if the TX FIFO underflows.
7 (0x07)	Asserts when a packet has been received with CRC OK. De-asserts when the first byte is read from the RX FIFO.
8 (0x08)	Reserved - used for test.
9 (0x09)	Clear channel assessment. High when RSSI level is below threshold (dependent on the current CCA_MODE setting).
10 (0x0A)	Lock detector output. The PLL is in lock if the lock detector output has a positive transition or is constantly logic high. To check for PLL lock the lock detector output should be used as an interrupt for the MCU.
11 (0x0B)	Serial Clock. Synchronous to the data in synchronous serial mode. In RX mode, data is set up on the falling edge by CC110L when GDOx_INV=0. In TX mode, data is sampled by CC110L on the rising edge of the serial clock when GDOx_INV=0.
12 (0x0C)	Serial Synchronous Data Output. Used for synchronous serial mode.
13 (0x0D)	Serial Data Output. Used for asynchronous serial mode.
14 (0x0E)	Carrier sense. High if RSSI level is above threshold. Cleared when entering IDLE mode.
15 (0x0F)	CRC_OK. The last CRC comparison matched. Cleared when entering/restarting RX mode.
16 (0x10) - 26 (0x1A)	Reserved - used for test.
27 (0x1B)	PA_PD. **Note**: PA_PD will have the same signal level in SLEEP and TX states. To control an external PA or RX/TX switch in applications where the SLEEP state is used it is recommended to use GDOx_CFGx=0x2F instead.
28 (0x1C)	LNA_PD. **Note:** LNA_PD will have the same signal level in SLEEP and RX states. To control an external LNA or RX/TX switch in applications where the SLEEP state is used it is recommended to use GDOx_CFGx=0x2F instead.
29 (0x1D) - 38 (0x26)	Reserved - used for test.
39 (0x27)	CLK_32k.
40 (0x28)	Reserved - used for test.
41 (0x29)	CHIP_RDYn.
42 (0x2A)	Reserved - used for test.
43 (0x2B)	XOSC_STABLE.
44 (0x2C) - 45 (0x2D)	Reserved - used for test.
46 (0x2E)	High impedance (3-state).
47 (0x2F)	HW to 0 (HW1 achieved by setting GDOx_INV=1). Can be used to control an external LNA/PA or RX/TX switch.

GDOx_CFG[5:0]	Description	
48 (0x30)	CLK_XOSC/1	**Note:** There are 3 GDO pins, but only one CLK_XOSC/n can be selected as an output at any time. If CLK_XOSC/n is to be monitored on one of the GDO pins, the other two GDO pins must be configured to values less than 0x30. The GDO0 default value is CLK_XOSC/192. To optimize RF performance, these signals should not be used while the radio is in RX or TX mode.
49 (0x31)	CLK_XOSC/1.5	
50 (0x32)	CLK_XOSC/2	
51 (0x33)	CLK_XOSC/3	
52 (0x34)	CLK_XOSC/4	
53 (0x35)	CLK_XOSC/6	
54 (0x36)	CLK_XOSC/8	
55 (0x37)	CLK_XOSC/12	
56 (0x38)	CLK_XOSC/16	
57 (0x39)	CLK_XOSC/24	
58 (0x3A)	CLK_XOSC/32	
59 (0x3B)	CLK_XOSC/48	
60 (0x3C)	CLK_XOSC/64	
61 (0x3D)	CLK_XOSC/96	
62 (0x3E)	CLK_XOSC/128	
63 (0x3F)	CLK_XOSC/192	

Table 36: GDOx Signal Selection (x = 0, 1, or 2)

25 Asynchronous and Synchronous Serial Operation

Several features and modes of operation have been included in the CC110L to provide backward compatibility with previous Chipcon products and other existing RF communication systems. For new systems, it is recommended to use the built-in packet handling features, as they can give more robust communication, significantly offload the microcontroller, and simplify software development.

25.1 Asynchronous Serial Operation

Asynchronous transfer is included in the CC110L for backward compatibility with systems that are already using the asynchronous data transfer.

When asynchronous transfer is enabled, all packet handling support is disabled and it is not possible to use Manchester encoding.

Asynchronous serial mode is enabled by setting `PKTCTRL0.PKT_FORMAT` to 3. Strobing `STX` will configure the GDO0 pin as data input (TX data) regardless of the content of the `IOCFG0` register. Data output can be on GDO0, GDO1, or GDO2. This is set by the `IOCFG0.GDO0_CFG`, `IOCFG1.GDO1_CFG` and `IOCFG2.GDO2_CFG` fields

The CC110L modulator samples the level of the asynchronous input 8 times faster than the programmed data rate. The timing requirement for the asynchronous stream is that the error in the bit period must be less than one eighth of the programmed data rate.

In asynchronous serial mode no data decision is done on-chip and the raw data is put on the data output line. When using asynchronous serial mode make sure the interfacing MCU does proper oversampling and that it can handle the jitter on the data output line. The MCU should tolerate a jitter of ±1/8 of a bit period as the data stream is time-discrete using 8 samples per bit.

In asynchronous serial mode there will be glitches of 37 - 38.5 ns duration (1/XOSC) occurring infrequently and with random periods. A simple RC filter can be added to the data output line between CC110L and the MCU to get rid of the 37 - 38.5 ns glitches if considered a problem. The filter 3 dB cut-off frequency needs to be high enough so that the data is not filtered and at the same time low enough to remove the glitch. As an example, for 2.4 kBaud data rate a 1 kΩ resistor and 2.7 nF capacitor can be used. This gives a 3 dB cut-off frequency of 59 kHz.

25.2 Synchronous Serial Operation

Setting PKTCTRL0.PKT_FORMAT to 1 enables synchronous serial mode. When using this mode, sync detection should be disabled together with CRC calculation (MDMCFG2.SYNC_MODE=000 and PKTCTRL0.CRC_EN=0). Infinite packet length mode should be used ($PKTCTRL0.LENGTH\_CONFIG=10_b$).

In synchronous serial mode, data is transferred on a two-wire serial interface. The CC110L provides a clock that is used to set up new data on the data input line or sample data on the data output line. Data input (TX data) is on the GDO0 pin. This pin will automatically be configured as an input when TX is active. The TX latency is 8 bits.The data output pin can be any of the GDO pins. This is set by the IOCFG0.GDO0_CFG, IOCFG1.GDO1_CFG, and IOCFG2.GDO2_CFG fields. The RX latency is 9 bits.

The MCU must handle preamble and sync word detection in software.

The MCU must handle preamble and sync word insertion/detection in software, together with CRC calculation and insertion.

26 System Considerations and Guidelines

26.1 SRD Regulations

International regulations and national laws regulate the use of radio receivers and transmitters. Short Range Devices (SRDs) for license free operation below 1 GHz are usually operated in the 315 MHz, 433 MHz, 868 MHz or 915 MHz frequency bands. The CC110L is specifically designed for such use with its 300 - 348 MHz, 387 - 464 MHz, and 779 - 928 MHz operating ranges. The most important regulations when using the CC110L in the 315 MHz, 433 MHz, 868 MHz, or 915 MHz frequency bands are EN 300 220 V2.3.1 (Europe) and FCC CFR47 Part 15 (USA).

For compliance with modulation bandwidth requirements under EN 300 220 V2.3.1 in the 863 to 870 MHz frequency range it is recommended to use a 26 MHz crystal for frequencies below 869 MHz and a 27 MHz crystal for frequencies above 869 MHz.

Please note that compliance with regulations is dependent on the complete system performance. It is the customer's responsibility to ensure that the system complies with regulations.

26.2 Frequency Hopping and Multi-Channel Systems

CC110L is highly suited for FHSS or multi-channel systems due to its agile frequency synthesizer and effective communication interface.

Charge pump current, VCO current, and VCO capacitance array calibration data is required for each frequency when implementing frequency hopping for CC110L. There are 3 ways of obtaining the calibration data from the chip:

1) Frequency hopping with calibration for each hop. The PLL calibration time is 712/724 µs (26 MHz crystal and TEST0 = 0x09/0B, see Table 30). The blanking interval between each frequency hop is then 787/799 µs.

2) Fast frequency hopping without calibration for each hop can be done by performing the necessary calibrating at startup and saving the resulting FSCAL3, FSCAL2, and FSCAL1 register values in MCU memory. The VCO capacitance calibration FSCAL1 register value must be found for each RF frequency to be used. The VCO current calibration value and the charge pump current calibration value available in FSCAL2 and FSCAL3 respectively are not dependent on the RF frequency, so the same value can therefore be used for all RF frequencies for these two registers. Between each frequency hop, the calibration process can then be replaced by writing the FSCAL3, FSCAL2 and FSCAL1 register values that corresponds to the next RF frequency. The PLL turn on time is approximately 75 µs (Table 29). The blanking interval between each frequency hop is then approximately 75 µs.

3) Run calibration on a single frequency at startup. Next write 0 to FSCAL3[5:4] to disable the charge pump calibration. After writing to FSCAL3[5:4], strobe SRX (or STX) with MCSM0.FS_AUTOCAL=1 for each new frequency hop. That is, VCO current and VCO capacitance calibration is done, but not charge pump current calibration. When charge pump current calibration is disabled the calibration time is reduced from 712/724 µs to 145/157 µs (26 MHz crystal and TEST0 = 0x09/0B, see Table 30). The blanking interval between each frequency hop is then 220/232 µs.

There is a trade off between blanking time and memory space needed for storing calibration data in non-volatile memory. Solution 2) above gives the shortest blanking interval, but requires more memory space to store calibration values. This solution also requires that the supply voltage and temperature do not vary much in order to have a robust solution. Solution 3) gives 567 µs smaller blanking interval than solution 1).

The recommended settings for TEST0.VCO_SEL_CAL_EN change with frequency. This means that one should always use SmartRF Studio [4] to get the correct settings for a specific frequency before doing a calibration, regardless of which calibration method is being used.

Note: The content in the TEST0 register is not retained in SLEEP state, thus it is necessary to re-write this register when returning from the SLEEP state.

26.3 Wideband Modulation when not Using Spread Spectrum

Digital modulation systems under FCC Section 15.247 include 2-FSK, GFSK, and 4-FSK modulation. A maximum peak output power of 1 W (+30 dBm) is allowed if the 6 dB bandwidth of the modulated signal exceeds 500 kHz. In addition, the peak power spectral density conducted to the antenna shall not be greater than +8 dBm in any 3 kHz band.

Operating at high data rates and frequency separation, the CC110L is suited for systems targeting compliance with digital modulation system as defined by FCC Section 15.247. An external power amplifier such as CC1190 [13] is needed to increase the output above +11 dBm. Please refer to DN006 [8] for further details concerning wideband modulation and CC110L.

26.4 Data Burst Transmissions

The high maximum data rate of CC110L opens up for burst transmissions. A low average data rate link (e.g. 10 kBaud) can be realized by using a higher over-the-air data rate. Buffering the data and transmitting in bursts at high data rate (e.g. 500 kBaud) will reduce the time in active mode, and hence also reduce the average current consumption significantly. Reducing the time in active mode will reduce the likelihood of collisions with other systems in the same frequency range.

Note: The sensitivity and thus transmission range is reduced for high data rate bursts compared to lower data rates.

26.5 Continuous Transmissions

In data streaming applications, the CC110L opens up for continuous transmissions at 500 kBaud effective data rate. As the modulation is done with a closed loop PLL, there is no limitation in the length of a transmission (open loop modulation used in some transceivers often prevents this kind of continuous data streaming and reduces the effective data rate).

26.6 Increasing Range

In some applications it may be necessary to extend the range. The CC1190 [13] is a range extender for 850-950 MHz RF transceivers, transmitters, and System-on-Chip devices from Texas Instruments. It increases the link budget by providing a power amplifier (PA) for increased output power, and a low-noise amplifier (LNA) with low noise figure for improved receiver sensitivity in addition to switches and RF matching for simple design of high performance wireless systems. Refer to

AN094 [14] and AN096 [15] for performance figures of the CC110L + CC1190 combination.

Figure 24 shows a simplified application circuit.

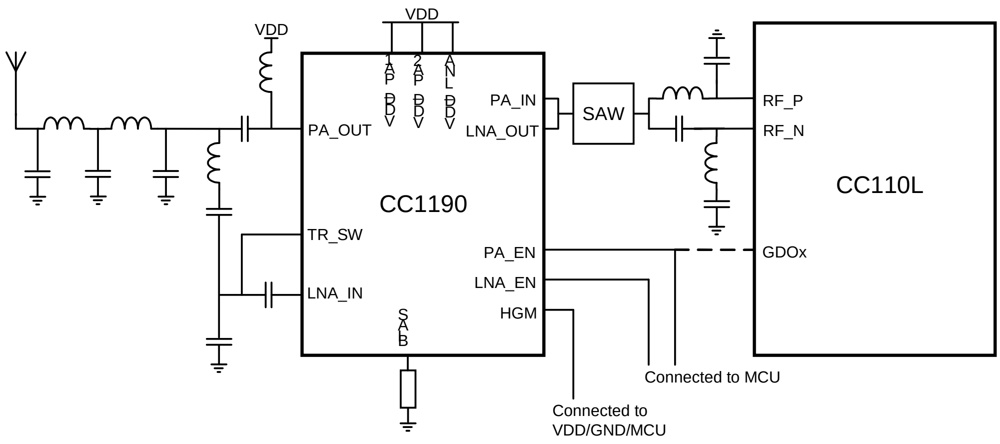


Figure 24: Simplified CC110L-CC1190 Application Circuit

27 Configuration Registers

The configuration of CC110L is done by programming 8-bit registers. The optimum configuration data based on selected system parameters are most easily found by using the SmartRF Studio software [4]. Complete descriptions of the registers are given in the following tables. After chip reset, all the registers have default values as shown in the tables. The optimum register setting might differ from the default value. After a reset, all registers that shall be different from the default value therefore needs to be programmed through the SPI interface.

There are 11 command strobe registers, listed in Table 37. Accessing these registers will initiate the change of an internal state or mode. There are 44 normal 8-bit configuration registers listed in Table 38 and SmartRF Studio [4] will provide recommended settings for these registers[2].

There are also 9 status registers that are listed in Table 39. These registers, which are read-only, contain information about the status of CC110L.

The two FIFOs are accessed through one 8-bit register. Write operations write to the TX FIFO, while read operations read from the RX FIFO.

During the header byte transfer and while writing data to a register or the TX FIFO, a status byte is returned on the SO line. This status byte is described in Table 20 on page 25.

Table 40 summarizes the SPI address space. The address to use is given by adding the base address to the left and the burst and read/write bits on the top. Note that the burst bit has different meaning for base addresses above and below 0x2F.

[2] Addresses marked as "Not Used" can be part of a burst access and one can write a dummy value to them. Addresses marked as "Reserved" must be configured according to SmartRF Studio [4]

Address	Strobe Name	Description
0x30	SRES	Reset chip.
0x31	SFSTXON	Enable and calibrate frequency synthesizer (if MCSM0.FS_AUTOCAL=1). If in RX (with CCA): Go to a wait state where only the synthesizer is running (for quick RX / TX turnaround).
0x32	SXOFF	Turn off crystal oscillator.
0x33	SCAL	Calibrate frequency synthesizer and turn it off. SCAL can be strobed from IDLE mode without setting manual calibration mode (MCSM0.FS_AUTOCAL=0)
0x34	SRX	In IDLE state: Enable RX. Perform calibration first if MCSM0.FS_AUTOCAL=1.
0x35	STX	In IDLE state: Enable TX. Perform calibration first if MCSM0.FS_AUTOCAL=1. If in RX state and CCA is enabled: Only go to TX if channel is clear.
0x36	SIDLE	Enter IDLE state
0x37 - 0x38	Reserved	
0x39	SPWD	Enter power down mode when CSn goes high.
0x3A	SFRX	Flush the RX FIFO buffer. Only issue SFRX in IDLE or RXFIFO_OVERFLOW states.
0x3B	SFTX	Flush the TX FIFO buffer. Only issue SFTX in IDLE or TXFIFO_UNDERFLOW states.
0x3C	Reserved	
0x3D	SNOP	No operation. May be used to get access to the chip status byte.

Table 37: Command Strobes

Address	Register	Description	Preserved in SLEEP State	Details on Page Number
0x00	IOCFG2	GDO2 output pin configuration	Yes	57
0x01	IOCFG1	GDO1 output pin configuration	Yes	57
0x02	IOCFG0	GDO0 output pin configuration	Yes	57
0x03	FIFOTHR	RX FIFO and TX FIFO thresholds	Yes	58
0x04	SYNC1	Sync word, high byte	Yes	59
0x05	SYNC0	Sync word, low byte	Yes	59
0x06	PKTLEN	Packet length	Yes	59
0x07	PKTCTRL1	Packet automation control	Yes	59
0x08	PKTCTRL0	Packet automation control	Yes	60
0x09	ADDR	Device address	Yes	60
0x0A	CHANNR	Channel number	Yes	60
0x0B	FSCTRL1	Frequency synthesizer control	Yes	60
0x0C	FSCTRL0	Frequency synthesizer control	Yes	61
0x0D	FREQ2	Frequency control word, high byte	Yes	61
0x0E	FREQ1	Frequency control word, middle byte	Yes	61
0x0F	FREQ0	Frequency control word, low byte	Yes	61
0x10	MDMCFG4	Modem configuration	Yes	61
0x11	MDMCFG3	Modem configuration	Yes	61
0x12	MDMCFG2	Modem configuration	Yes	62
0x13	MDMCFG1	Modem configuration	Yes	63
0x14	MDMCFG0	Modem configuration	Yes	63
0x15	DEVIATN	Modem deviation setting	Yes	64
0x16	MCSM2	Main Radio Control State Machine configuration	Yes	64
0x17	MCSM1	Main Radio Control State Machine configuration	Yes	65
0x18	MCSM0	Main Radio Control State Machine configuration	Yes	66
0x19	FOCCFG	Frequency Offset Compensation configuration	Yes	67
0x1A	BSCFG	Bit Synchronization configuration	Yes	68
0x1B	AGCTRL2	AGC control	Yes	69
0x1C	AGCTRL1	AGC control	Yes	70
0x1D	AGCTRL0	AGC control	Yes	71
0x1E - 0x1F	Not Used			
0x20	RESERVED		Yes	71
0x21	FREND1	Front end RX configuration	Yes	72
0x22	FREND0	Front end TX configuration	Yes	72
0x23	FSCAL3	Frequency synthesizer calibration	Yes	72
0x24	FSCAL2	Frequency synthesizer calibration	Yes	72
0x25	FSCAL1	Frequency synthesizer calibration	Yes	72
0x26	FSCAL0	Frequency synthesizer calibration	Yes	73
0x27 - 0x28	Not Used			
0x29 - 0x2B	RESERVED		No	73
0x2C	TEST2	Various test settings	No	73
0x2D	TEST1	Various test settings	No	73
0x2E	TEST0	Various test settings	No	73

Table 38: Configuration Registers Overview

Address	Register	Description	Details on page number
0x30 (0xF0)	PARTNUM	Part number for CC110L	74
0x31 (0xF1)	VERSION	Current version number	74
0x32 (0xF2)	FREQEST	Frequency Offset Estimate	74
0x33 (0xF3)	CRC_REG	CRC OK	74
0x34 (0xF4)	RSSI	Received signal strength indication	74
0x35 (0xF5)	MARCSTATE	Control state machine state	75
0x36 - 0x37 (0xF6 – 0xF7)	Reserved		
0x38 (0xF8)	PKTSTATUS	Current GDOx status and packet status	76
0x39 (0xF9)	Reserved		
0x3A (0xFA)	TXBYTES	Underflow and number of bytes in the TX FIFO	76
0x3B (0xFB)	RXBYTES	Overflow and number of bytes in the RX FIFO	76
0x3C - 0x3D (0xFC - 0xFD)	Reserved		

Table 39: Status Registers Overview

	Write		Read		
	Single Byte	Burst	Single Byte	Burst	
	+0x00	+0x40	+0x80	+0xC0	
0x00	IOCFG2				R/W configuration registers, burst access possible
0x01	IOCFG1				
0x02	IOCFG0				
0x03	FIFOTHR				
0x04	SYNC1				
0x05	SYNC0				
0x06	PKTLEN				
0x07	PKTCTRL1				
0x08	PKTCTRL0				
0x09	ADDR				
0x0A	CHANNR				
0x0B	FSCTRL1				
0x0C	FSCTRL0				
0x0D	FREQ2				
0x0E	FREQ1				
0x0F	FREQ0				
0x10	MDMCFG4				
0x11	MDMCFG3				
0x12	MDMCFG2				
0x13	MDMCFG1				
0x14	MDMCFG0				
0x15	DEVIATN				
0x16	MCSM2				
0x17	MCSM1				
0x18	MCSM0				
0x19	FOCCFG				
0x1A	BSCFG				
0x1B	AGCCTRL2				
0x1C	AGCCTRL1				
0x1D	AGCCTRL0				
0x1E	Not Used				
0x1F	Not Used				
0x20	RESERVED				
0x21	FREND1				
0x22	FREND0				
0x23	FSCAL3				
0x24	FSCAL2				
0x25	FSCAL1				
0x26	FSCAL0				
0x27	Not Used				
0x28	Not Used				
0x29	RESERVED				
0x2A	RESERVED				
0x2B	RESERVED				
0x2C	TEST2				
0x2D	TEST1				
0x2E	TEST0				
0x2F	Not Used				
0x30	SRES		SRES	PARTNUM	Command Strobes, Status registers (read only) and multi byte registers
0x31	SFSTXON		SFSTXON	VERSION	
0x32	SXOFF		SXOFF	FREQEST	
0x33	SCAL		SCAL	CRC_REG	
0x34	SRX		SRX	RSSI	
0x35	STX		STX	MARCSTATE	
0x36	SIDLE		SIDLE	Reserved	
0x37	Reserved		Reserved	Reserved	
0x38	Reserved		Reserved	PKTSTATUS	
0x39	SPWD		SPWD	Reserved	
0x3A	SFRX		SFRX	TXBYTES	
0x3B	SFTX		SFTX	RXBYTES	
0x3C	Reserved		Reserved	Reserved	
0x3D	SNOP		SNOP	Reserved	
0x3E	PATABLE	PATABLE	PATABLE	PATABLE	
0x3F	TX FIFO	TX FIFO	RX FIFO	RX FIFO	

Table 40: SPI Address Space

27.1 Configuration Register Details - Registers with preserved values in SLEEP state

0x00: IOCFG2 - GDO2 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6	GDO2_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO2_CFG[5:0]	41 (101001)	R/W	Default is CHP_RDYn (See Table 36 on page 49).

0x01: IOCFG1 - GDO1 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7	GDO_DS	0	R/W	Set high (1) or low (0) output drive strength on the GDO pins.
6	GDO1_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO1_CFG[5:0]	46 (101110)	R/W	Default is 3-state (See Table 36 on page 49).

0x02: IOCFG0 - GDO0 Output Pin Configuration

Bit	Field Name	Reset	R/W	Description
7		0	R/W	Use setting from SmartRF Studio [4]
6	GDO0_INV	0	R/W	Invert output, i.e. select active low (1) / high (0)
5:0	GDO0_CFG[5:0]	63 (0x3F)	R/W	Default is CLK_XOSC/192 (See Table 36 on page 49). It is recommended to disable the clock output in initialization, in order to optimize RF performance.

0x03: FIFOTHR - RX FIFO and TX FIFO Thresholds

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td>7</td><td></td><td>0</td><td>R/W</td><td colspan="3">Use setting from SmartRF Studio [4]</td></tr>
<tr><td>6</td><td>ADC_RETENTION</td><td>0</td><td>R/W</td><td colspan="3">0: TEST1 = 0x31 and TEST2= 0x88 when waking up from SLEEP
1: TEST1 = 0x35 and TEST2 = 0x81 when waking up from SLEEP
Note that the changes in the TEST registers due to the ADC_RETENTION bit setting are only seen INTERNALLY in the analog part. The values read from the TEST registers when waking up from SLEEP mode will always be the reset value.
The ADC_RETENTION bit should be set to 1before going into SLEEP mode if settings with an RX filter bandwidth below 325 kHz are wanted at time of wake-up.</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">CLOSE_IN_RX[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="3">For more details, please see DN010 [5]</td></tr>
<tr><td>Setting</td><td colspan="2">RX Attenuation, Typical Values</td></tr>
<tr><td>0 (00)</td><td colspan="2">0 dB</td></tr>
<tr><td>1 (01)</td><td colspan="2">6 dB</td></tr>
<tr><td>2 (10)</td><td colspan="2">12 dB</td></tr>
<tr><td>3 (11)</td><td colspan="2">18 dB</td></tr>
<tr><td rowspan="18">3:0</td><td rowspan="18">FIFO_THR[3:0]</td><td rowspan="18">7 (0111)</td><td rowspan="18">R/W</td><td colspan="3">Set the threshold for the RX FIFO and TX FIFO. The threshold is exceeded when the number of bytes in the FIFO is equal to or higher than the threshold value.</td></tr>
<tr><td>Setting</td><td>Bytes in RX FIFO</td><td>Bytes in TX FIFO</td></tr>
<tr><td>0 (0000)</td><td>4</td><td>61</td></tr>
<tr><td>1 (0001)</td><td>8</td><td>57</td></tr>
<tr><td>2 (0010)</td><td>12</td><td>53</td></tr>
<tr><td>3 (0011)</td><td>16</td><td>49</td></tr>
<tr><td>4 (0100)</td><td>20</td><td>45</td></tr>
<tr><td>5 (0101)</td><td>24</td><td>41</td></tr>
<tr><td>6 (0110)</td><td>28</td><td>37</td></tr>
<tr><td>7 (0111)</td><td>32</td><td>33</td></tr>
<tr><td>8 (1000)</td><td>36</td><td>29</td></tr>
<tr><td>9 (1001)</td><td>40</td><td>25</td></tr>
<tr><td>10 (1010)</td><td>44</td><td>21</td></tr>
<tr><td>11 (1011)</td><td>48</td><td>17</td></tr>
<tr><td>12 (1100)</td><td>52</td><td>13</td></tr>
<tr><td>13 (1101)</td><td>56</td><td>9</td></tr>
<tr><td>14 (1110)</td><td>60</td><td>5</td></tr>
<tr><td>15 (1111)</td><td>64</td><td>1</td></tr>
</table>

0x04: SYNC1 - Sync Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[15:8]	211 (0xD3)	R/W	8 MSB of 16-bit sync word

0x05: SYNC0 - Sync Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	SYNC[7:0]	145 (0x91)	R/W	8 LSB of 16-bit sync word

0x06: PKTLEN - Packet Length

Bit	Field Name	Reset	R/W	Description
7:0	PACKET_LENGTH	255 (0xFF)	R/W	Indicates the packet length when fixed packet length mode is enabled. If variable packet length mode is used, this value indicates the maximum packet length allowed. This value must be different from 0.

0x07: PKTCTRL1 - Packet Automation Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="2">Description</th></tr>
<tr><td>7:5</td><td></td><td>0 (000)</td><td>R/W</td><td colspan="2">Use setting from SmartRF Studio [4]</td></tr>
<tr><td>4</td><td></td><td>0</td><td>R0</td><td colspan="2">Not Used.</td></tr>
<tr><td>3</td><td>CRC_AUTOFLUSH</td><td>0</td><td>R/W</td><td colspan="2">Enable automatic flush of RX FIFO when CRC is not OK. This requires that only one packet is in the RX FIFO and that packet length is limited to the RX FIFO size.</td></tr>
<tr><td>2</td><td>APPEND_STATUS</td><td>1</td><td>R/W</td><td colspan="2">When enabled, two status bytes will be appended to the payload of the packet. The status bytes contain the RSSI value, as well as CRC OK.</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">ADR_CHK[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="2">Controls address check configuration of received packages.</td></tr>
<tr><td>Setting</td><td>Address check configuration</td></tr>
<tr><td>0 (00)</td><td>No address check</td></tr>
<tr><td>1 (01)</td><td>Address check, no broadcast</td></tr>
<tr><td>2 (10)</td><td>Address check and 0 (0x00) broadcast</td></tr>
<tr><td>3 (11)</td><td>Address check and 0 (0x00) and 255 (0xFF) broadcast</td></tr>
</table>

0x08: PKTCTRL0 - Packet Automation Control

Bit	Field Name	Reset	R/W	Description	
7			R0	Not used	
6		1	R/W	Use setting from SmartRF Studio [4]	
5:4	PKT_FORMAT[1:0]	0 (00)	R/W	Format of RX data	
				Setting	Packet format
				0 (00)	Normal mode, use FIFOs for RX and TX
				1 (01)	Synchronous serial mode. Data in on GDO0 and data out on either of the GDOx pins
				2 (10)	Random TX mode; sends random data using PN9 generator. Used for test. Works as normal mode, setting 0 (00), in RX
				3 (11)	Asynchronous serial mode. Data in on GDO0 and data out on either of the GDOx pins
3		0	R0	Not used	
2	CRC_EN	1	R/W	1: CRC calculation enabled 0: CRC calculation disabled	
1:0	LENGTH_CONFIG[1:0]	1 (01)	R/W	Configure the packet length	
				Setting	Packet length configuration
				0 (00)	Fixed packet length mode. Length configured in `PKTLEN` register
				1 (01)	Variable packet length mode. Packet length configured by the first byte after sync word
				2 (10)	Infinite packet length mode
				3 (11)	Reserved

0x09: ADDR - Device Address

Bit	Field Name	Reset	R/W	Description
7:0	DEVICE_ADDR[7:0]	0 (0x00)	R/W	Address used for packet filtration. Optional broadcast addresses are 0 (0x00) and 255 (0xFF).

0x0A: CHANNR - Channel Number

Bit	Field Name	Reset	R/W	Description
7:0	CHAN[7:0]	0 (0x00)	R/W	The 8-bit unsigned channel number, which is multiplied by the channel spacing setting and added to the base frequency.

0x0B: FSCTRL1 - Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5		0	R/W	Use setting from SmartRF Studio [4]
4:0	FREQ_IF[4:0]	15 (01111)	R/W	The desired IF frequency to employ in RX. Subtracted from FS base frequency in RX and controls the digital complex mixer in the demodulator. $f_{IF} = \frac{f_{XOSC}}{2^{10}} \cdot FREQ\_IF$ The default value gives an IF frequency of 381kHz, assuming a 26.0 MHz crystal.

0x0C: FSCTRL0 - Frequency Synthesizer Control

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF[7:0]	0 (0x00)	R/W	Frequency offset added to the base frequency before being used by the frequency synthesizer. (2s-complement). Resolution is $F_{XTAL}/2^{14}$ (1.59kHz-1.65kHz); range is ±202 kHz to ±210 kHz, dependent of XTAL frequency.

0x0D: FREQ2 - Frequency Control Word, High Byte

Bit	Field Name	Reset	R/W	Description
7:6	FREQ[23:22]	0 (00)	R	`FREQ[23:22]` is always 0 (the `FREQ2` register is less than 36 with 26 - 27 MHz crystal)
5:0	FREQ[21:16]	30 (011110)	R/W	`FREQ[23:0]` is the base frequency for the frequency synthesiser in increments of $f_{XOSC}/2^{16}$. $f_{carrier} = \frac{f_{XOSC}}{2^{16}} \cdot FREQ[23:0]$

0x0E: FREQ1 - Frequency Control Word, Middle Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[15:8]	196 (0xC4)	R/W	Ref. `FREQ2` register

0x0F: FREQ0 - Frequency Control Word, Low Byte

Bit	Field Name	Reset	R/W	Description
7:0	FREQ[7:0]	236 (0xEC)	R/W	Ref. `FREQ2` register

0x10: MDMCFG4 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:6	CHANBW_E[1:0]	2 (10)	R/W	
5:4	CHANBW_M[1:0]	0 (00)	R/W	Sets the decimation ratio for the delta-sigma ADC input stream and thus the channel bandwidth. $BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW\_M) \cdot 2^{CHANBW\_E}}$ The default values give 203 kHz channel filter bandwidth, assuming a 26.0 MHz crystal.
3:0	DRATE_E[3:0]	12 (1100)	R/W	The exponent of the user specified symbol rate

0x11: MDMCFG3 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	DRATE_M[7:0]	34 (0x22)	R/W	The mantissa of the user specified symbol rate. The symbol rate is configured using an unsigned, floating-point number with 9-bit mantissa and 4-bit exponent. The 9th bit is a hidden '1'. The resulting data rate is: $R_{DATA} = \frac{(256 + DRATE\_M) \cdot 2^{DRATE\_E}}{2^{28}} \cdot f_{XOSC}$ The default values give a data rate of 115.051 kBaud (closest setting to 115.2 kBaud), assuming a 26.0 MHz crystal.

0x12: MDMCFG2 - Modem Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td>DEM_DCFILT_OFF</td><td>0</td><td>R/W</td><td colspan="2">Disable digital DC blocking filter before demodulator.
0 = Enable (better sensitivity)
1 = Disable (current optimized). Only for data rates ≤ 250 kBaud
The recommended IF frequency changes when the DC blocking is disabled. Please use SmartRF Studio [4] to calculate correct register setting.</td></tr>
<tr><td rowspan="11">6:4</td><td rowspan="11">MOD_FORMAT[2:0]</td><td rowspan="11">0 (000)</td><td rowspan="11">R/W</td><td colspan="2">The modulation format of the radio signal</td></tr>
<tr><td>Setting</td><td>Modulation format</td></tr>
<tr><td>0 (000)</td><td>2-FSK</td></tr>
<tr><td>1 (001)</td><td>GFSK</td></tr>
<tr><td>2 (010)</td><td>Reserved</td></tr>
<tr><td>3 (011)</td><td>OOK</td></tr>
<tr><td>4 (100)</td><td>4-FSK</td></tr>
<tr><td>5 (101)</td><td>Reserved</td></tr>
<tr><td>6 (110)</td><td>Reserved</td></tr>
<tr><td>7 (111)</td><td>Reserved</td></tr>
<tr><td colspan="2">4-FSK modulation cannot be used together with Manchester encoding</td></tr>
<tr><td>3</td><td>MANCHESTER_EN</td><td>0</td><td>R/W</td><td colspan="2">Enables Manchester encoding/decoding.
0 = Disable
1 = Enable
Manchester encoding cannot be used when using asynchronous serial mode or 4-FSK modulation</td></tr>
<tr><td rowspan="10">2:0</td><td rowspan="10">SYNC_MODE[2:0]</td><td rowspan="10">2 (010)</td><td rowspan="10">R/W</td><td colspan="2">Combined sync-word qualifier mode.
The values 0 and 4 disables preamble and sync word detection
The values 1, 2, 5, and 6 enables 16-bit sync word detection. Only 15 of 16 bits need to match when using setting 1 or 5. The values 3 and 7 enables 32-bits sync word detection (only 30 of 32 bits need to match).</td></tr>
<tr><td>Setting</td><td>Sync-word qualifier mode</td></tr>
<tr><td>0 (000)</td><td>No preamble/sync</td></tr>
<tr><td>1 (001)</td><td>15/16 sync word bits detected</td></tr>
<tr><td>2 (010)</td><td>16/16 sync word bits detected</td></tr>
<tr><td>3 (011)</td><td>30/32 sync word bits detected</td></tr>
<tr><td>4 (100)</td><td>No preamble/sync, carrier-sense above threshold</td></tr>
<tr><td>5 (101)</td><td>15/16 + carrier-sense above threshold</td></tr>
<tr><td>6 (110)</td><td>16/16 + carrier-sense above threshold</td></tr>
<tr><td>7 (111)</td><td>30/32 + carrier-sense above threshold</td></tr>
</table>

0x13: MDMCFG1 - Modem Configuration

Bit	Field Name	Reset	R/W	Description	
7		0	R/W	Use setting from SmartRF Studio [4]	
6:4	NUM_PREAMBLE[2:0]	2 (010)	R/W	Sets the minimum number of preamble bytes to be transmitted	
				Setting	Number of preamble bytes
				0 (000)	2
				1 (001)	3
				2 (010)	4
				3 (011)	6
				4 (100)	8
				5 (101)	12
				6 (110)	16
				7 (111)	24
3:2			R0	Not used	
1:0	CHANSPC_E[1:0]	2 (10)	R/W	2 bit exponent of channel spacing	

0x14: MDMCFG0 - Modem Configuration

Bit	Field Name	Reset	R/W	Description
7:0	CHANSPC_M[7:0]	248 (0xF8)	R/W	8-bit mantissa of channel spacing. The channel spacing is multiplied by the channel number CHAN and added to the base frequency. It is unsigned and has the format: $\Delta f_{CHANNEL} = \frac{f_{XOSC}}{2^{18}} \cdot (256 + CHANSPC\_M) \cdot 2^{CHANSPC\_E}$ The default values give 199.951 kHz channel spacing (the closest setting to 200 kHz), assuming 26.0 MHz crystal frequency.

0x15: DEVIATN - Modem Deviation Setting

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td></td><td></td><td>R0</td><td colspan="2">Not used.</td></tr>
<tr><td>6:4</td><td>DEVIATION_E[2:0]</td><td>4 (100)</td><td>R/W</td><td colspan="2">Deviation exponent.</td></tr>
<tr><td>3</td><td></td><td></td><td>R0</td><td colspan="2">Not used.</td></tr>
<tr><td rowspan="7">2:0</td><td rowspan="7">DEVIATION_M[2:0]</td><td rowspan="7">7 (111)</td><td rowspan="7">R/W</td><td colspan="2">RX</td></tr>
<tr><td>2-FSK/
GFSK/
4-FSK</td><td>Specifies the expected frequency deviation of incoming signal, must be approximately right for demodulation to be performed reliably and robustly.</td></tr>
<tr><td>OOK</td><td>This setting has no effect.</td></tr>
<tr><td colspan="2">TX</td></tr>
<tr><td>2-FSK/
GFSK/
4-FSK</td><td>Specifies the nominal frequency deviation from the carrier for
a ‘0’ (-DEVIATN) and ‘1’ (+DEVIATN) in a mantissa-exponent format, interpreted as a 4-bit value with MSB implicit 1. The resulting frequency deviation is given by:
$f_{dev} = \frac{f_{xosc}}{2^{17}} \cdot (8 + DEVIATION\_M) \cdot 2^{DEVIATION\_E}$
The default values give ±47.607 kHz deviation assuming 26.0 MHz crystal frequency.</td></tr>
<tr><td>OOK</td><td>This setting has no effect</td></tr>
</table>

0x16: MCSM2 - Main Radio Control State Machine Configuration

Bit	Field Name	Reset	R/W	Description
7:5			R0	Not used
4	RX_TIME_RSSI	0	R/W	Direct RX termination based on RSSI measurement (carrier sense). For OOK modulation, RX times out if there is no carrier sense in the first 8 symbol periods.
3:0		7 (0111)	R/W	Use setting from SmartRF Studio [4]

0x17: MCSM1 - Main Radio Control State Machine Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="2">Description</th></tr>
<tr><td>7:6</td><td></td><td></td><td>R0</td><td colspan="2">Not used</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">CCA_MODE</td><td rowspan="6">3 (11)</td><td rowspan="6">R/W</td><td colspan="2">Selects CCA_MODE; Reflected in CCA signal</td></tr>
<tr><td>Setting</td><td>Clear channel indication</td></tr>
<tr><td>0 (00)</td><td>Always</td></tr>
<tr><td>1 (01)</td><td>If RSSI below threshold</td></tr>
<tr><td>2 (10)</td><td>Unless currently receiving a packet</td></tr>
<tr><td>3 (11)</td><td>If RSSI below threshold unless currently receiving a packet</td></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">RXOFF_MODE[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="2">Select what should happen when a packet has been received.</td></tr>
<tr><td>Setting</td><td>Next state after finishing packet reception</td></tr>
<tr><td>0 (00)</td><td>IDLE</td></tr>
<tr><td>1 (01)</td><td>FSTXON</td></tr>
<tr><td>2 (10)</td><td>TX</td></tr>
<tr><td>3 (11)</td><td>Stay in RX</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">TXOFF_MODE[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="2">Select what should happen when a packet has been sent</td></tr>
<tr><td>Setting</td><td>Next state after finishing packet transmission</td></tr>
<tr><td>0 (00)</td><td>IDLE</td></tr>
<tr><td>1 (01)</td><td>FSTXON</td></tr>
<tr><td>2 (10)</td><td>Stay in TX (start sending preamble)</td></tr>
<tr><td>3 (11)</td><td>RX</td></tr>
</table>

0x18: MCSM0 - Main Radio Control State Machine Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td>7:6</td><td></td><td></td><td>R0</td><td colspan="3">Not used</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">FS_AUTOCAL[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="3">Automatically calibrate when going to RX or TX, or back to IDLE</td></tr>
<tr><td>Setting</td><td colspan="2">When to perform automatic calibration</td></tr>
<tr><td>0 (00)</td><td colspan="2">Never (manually calibrate using SCAL strobe)</td></tr>
<tr><td>1 (01)</td><td colspan="2">When going from IDLE to RX or TX (or FSTXON)</td></tr>
<tr><td>2 (10)</td><td colspan="2">When going from RX or TX back to IDLE automatically</td></tr>
<tr><td>3 (11)</td><td colspan="2">Every 4^{th} time when going from RX or TX to IDLE automatically</td></tr>
<tr><td rowspan="7">3:2</td><td rowspan="7">PO_TIMEOUT</td><td rowspan="7">1 (01)</td><td rowspan="7">R/W</td><td colspan="3">Programs the number of times the six-bit ripple counter must expire after the XOSC has settled before CHP_RDYn goes low. [3]

If XOSC is on (stable) during power-down, PO_TIMEOUT shall be set so that the regulated digital supply voltage has time to stabilize before CHP_RDYn goes low (PO_TIMEOUT=2 recommended). Typical start-up time for the voltage regulator is 50 µs.

For robust operation it is recommended to use PO_TIMEOUT = 2 or 3 when XOSC is off during power-down.</td></tr>
<tr><td>Setting</td><td>Expire count</td><td>Timeout after XOSC start</td></tr>
<tr><td>0 (00)</td><td>1</td><td>Approx. 2.3 - 2.4 µs</td></tr>
<tr><td>1 (01)</td><td>16</td><td>Approx. 37 - 39 µs</td></tr>
<tr><td>2 (10)</td><td>64</td><td>Approx. 149 - 155 µs</td></tr>
<tr><td>3 (11)</td><td>256</td><td>Approx. 597 - 620 µs</td></tr>
<tr><td colspan="3">Exact timeout depends on crystal frequency.</td></tr>
<tr><td>1</td><td></td><td>0</td><td>R/W</td><td colspan="3">Use setting from SmartRF Studio [4]</td></tr>
<tr><td>0</td><td>XOSC_FORCE_ON</td><td>0</td><td>R/W</td><td colspan="3">Force the XOSC to stay on in the SLEEP state.</td></tr>
</table>

[3] Note that the XOSC_STABLE signal will be asserted at the same time as the CHIP_RDYn signal; i.e. the PO_TIMEOUT delays both signals and does not insert a delay between the signals.

0x19: FOCCFG - Frequency Offset Compensation Configuration

Bit	Field Name	Reset	R/W	Description	
7:6			R0	Not used	
5	FOC_BS_CS_GATE	1	R/W	If set, the demodulator freezes the frequency offset compensation and clock recovery feedback loops until the CS signal goes high.	
4:3	FOC_PRE_K[1:0]	2 (10)	R/W	The frequency compensation loop gain to be used before a sync word is detected.	
				Setting	Freq. compensation loop gain before sync word
				0 (00)	*K*
				1 (01)	2*K*
				2 (10)	3*K*
				3 (11)	4*K*
2	FOC_POST_K	1	R/W	The frequency compensation loop gain to be used after a sync word is detected.	
				Setting	Freq. compensation loop gain after sync word
				0	Same as FOC_PRE_K
				1	*K*/2
1:0	FOC_LIMIT[1:0]	2 (10)	R/W	The saturation point for the frequency offset compensation algorithm:	
				Setting	Saturation point (max compensated offset)
				0 (00)	±0 (no frequency offset compensation)
				1 (01)	$\pm BW_{CHAN}/8$
				2 (10)	$\pm BW_{CHAN}/4$
				3 (11)	$\pm BW_{CHAN}/2$
				Frequency offset compensation is not supported for OOK. Always use FOC_LIMIT=0 with this modulation format.	

0x1A: BSCFG - Bit Synchronization Configuration

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="2">Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">BS_PRE_KI[1:0]</td><td rowspan="6">1 (01)</td><td rowspan="6">R/W</td><td colspan="2">The clock recovery feedback loop integral gain to be used before a sync word is detected (used to correct offsets in data rate):</td></tr>
<tr><td>Setting</td><td>Clock recovery loop integral gain before sync word</td></tr>
<tr><td>0 (00)</td><td>K_I</td></tr>
<tr><td>1 (01)</td><td>$2K_I$</td></tr>
<tr><td>2 (10)</td><td>$3K_I$</td></tr>
<tr><td>3 (11)</td><td>$4K_I$</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">BS_PRE_KP[1:0]</td><td rowspan="6">2 (10)</td><td rowspan="6">R/W</td><td colspan="2">The clock recovery feedback loop proportional gain to be used before a sync word is detected.</td></tr>
<tr><td>Setting</td><td>Clock recovery loop proportional gain before sync word</td></tr>
<tr><td>0 (00)</td><td>K_P</td></tr>
<tr><td>1 (01)</td><td>$2K_P$</td></tr>
<tr><td>2 (10)</td><td>$3K_P$</td></tr>
<tr><td>3 (11)</td><td>$4K_P$</td></tr>
<tr><td rowspan="4">3</td><td rowspan="4">BS_POST_KI</td><td rowspan="4">1</td><td rowspan="4">R/W</td><td colspan="2">The clock recovery feedback loop integral gain to be used after a sync word is detected.</td></tr>
<tr><td>Setting</td><td>Clock recovery loop integral gain after sync word</td></tr>
<tr><td>0</td><td>Same as BS_PRE_KI</td></tr>
<tr><td>1</td><td>$K_I/2$</td></tr>
<tr><td rowspan="4">2</td><td rowspan="4">BS_POST_KP</td><td rowspan="4">1</td><td rowspan="4">R/W</td><td colspan="2">The clock recovery feedback loop proportional gain to be used after a sync word is detected.</td></tr>
<tr><td>Setting</td><td>Clock recovery loop proportional gain after sync word</td></tr>
<tr><td>0</td><td>Same as BS_PRE_KP</td></tr>
<tr><td>1</td><td>K_P</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">BS_LIMIT[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="2">The saturation point for the data rate offset compensation algorithm:</td></tr>
<tr><td>Setting</td><td>Data rate offset saturation (max data rate difference)</td></tr>
<tr><td>0 (00)</td><td>±0 (No data rate offset compensation performed)</td></tr>
<tr><td>1 (01)</td><td>±3.125 % data rate offset</td></tr>
<tr><td>2 (10)</td><td>±6.25 % data rate offset</td></tr>
<tr><td>3 (11)</td><td>±12.5 % data rate offset</td></tr>
</table>

0x1B: AGCCTRL2 - AGC Control

Bit	Field Name	Reset	R/W	Description	
7:6	MAX_DVGA_GAIN[1:0]	0 (00)	R/W	Reduces the maximum allowable DVGA gain.	
				Setting	Allowable DVGA settings
				0 (00)	All gain settings can be used
				1 (01)	The highest gain setting cannot be used
				2 (10)	The 2 highest gain settings cannot be used
				3 (11)	The 3 highest gain settings cannot be used
5:3	MAX_LNA_GAIN[2:0]	0 (000)	R/W	Sets the maximum allowable LNA + LNA 2 gain relative to the maximum possible gain.	
				Setting	Maximum allowable LNA + LNA 2 gain
				0 (000)	Maximum possible LNA + LNA 2 gain
				1 (001)	Approx. 2.6 dB below maximum possible gain
				2 (010)	Approx. 6.1 dB below maximum possible gain
				3 (011)	Approx. 7.4 dB below maximum possible gain
				4 (100)	Approx. 9.2 dB below maximum possible gain
				5 (101)	Approx. 11.5 dB below maximum possible gain
				6 (110)	Approx. 14.6 dB below maximum possible gain
				7 (111)	Approx. 17.1 dB below maximum possible gain
2:0	MAGN_TARGET[2:0]	3 (011)	R/W	These bits set the target value for the averaged amplitude from the digital channel filter (1 LSB = 0 dB).	
				Setting	Target amplitude from channel filter
				0 (000)	24 dB
				1 (001)	27 dB
				2 (010)	30 dB
				3 (011)	33 dB
				4 (100)	36 dB
				5 (101)	38 dB
				6 (110)	40 dB
				7 (111)	42 dB

0x1C: AGCCTRL1 - AGC Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="2">Description</th></tr>
<tr><td>7</td><td></td><td></td><td>R0</td><td colspan="2">Not used</td></tr>
<tr><td>6</td><td>AGC_LNA_PRIORITY</td><td>1</td><td>R/W</td><td colspan="2">Selects between two different strategies for LNA and LNA 2 gain adjustment. When 1, the LNA gain is decreased first. When 0, the LNA 2 gain is decreased to minimum before decreasing LNA gain.</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">CARRIER_SENSE_REL_THR[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="2">Sets the relative change threshold for asserting carrier sense</td></tr>
<tr><td>Setting</td><td>Carrier sense relative threshold</td></tr>
<tr><td>0 (00)</td><td>Relative carrier sense threshold disabled</td></tr>
<tr><td>1 (01)</td><td>6 dB increase in RSSI value</td></tr>
<tr><td>2 (10)</td><td>10 dB increase in RSSI value</td></tr>
<tr><td>3 (11)</td><td>14 dB increase in RSSI value</td></tr>
<tr><td rowspan="10">3:0</td><td rowspan="10">CARRIER_SENSE_ABS_THR[3:0]</td><td rowspan="10">0 (0000)</td><td rowspan="10">R/W</td><td colspan="2">Sets the absolute RSSI threshold for asserting carrier sense. The 2-complement signed threshold is programmed in steps of 1 dB and is relative to the MAGN_TARGET setting.</td></tr>
<tr><td>Setting</td><td>Carrier sense absolute threshold
(Equal to channel filter amplitude when AGC has not decreased gain)</td></tr>
<tr><td>-8 (1000)</td><td>Absolute carrier sense threshold disabled</td></tr>
<tr><td>-7 (1001)</td><td>7 dB below MAGN_TARGET setting</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>-1 (1111)</td><td>1 dB below MAGN_TARGET setting</td></tr>
<tr><td>0 (0000)</td><td>At MAGN_TARGET setting</td></tr>
<tr><td>1 (0001)</td><td>1 dB above MAGN_TARGET setting</td></tr>
<tr><td>…</td><td>…</td></tr>
<tr><td>7 (0111)</td><td>7 dB above MAGN_TARGET setting</td></tr>
</table>

0x1D: AGCCTRL0 - AGC Control

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">HYST_LEVEL[1:0]</td><td rowspan="6">2 (10)</td><td rowspan="6">R/W</td><td colspan="3">Sets the level of hysteresis on the magnitude deviation (internal AGC signal that determine gain changes).</td></tr>
<tr><td>Setting</td><td colspan="2">Description</td></tr>
<tr><td>0 (00)</td><td colspan="2">No hysteresis, small symmetric dead zone, high gain</td></tr>
<tr><td>1 (01)</td><td colspan="2">Low hysteresis, small asymmetric dead zone, medium gain</td></tr>
<tr><td>2 (10)</td><td colspan="2">Medium hysteresis, medium asymmetric dead zone, medium gain</td></tr>
<tr><td>3 (11)</td><td colspan="2">Large hysteresis, large asymmetric dead zone, low gain</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">WAIT_TIME[1:0]</td><td rowspan="6">1 (01)</td><td rowspan="6">R/W</td><td colspan="3">Sets the number of channel filter samples from a gain adjustment has been made until the AGC algorithm starts accumulating new samples.</td></tr>
<tr><td>Setting</td><td colspan="2">Channel filter samples</td></tr>
<tr><td>0 (00)</td><td colspan="2">8</td></tr>
<tr><td>1 (01)</td><td colspan="2">16</td></tr>
<tr><td>2 (10)</td><td colspan="2">24</td></tr>
<tr><td>3 (11)</td><td colspan="2">32</td></tr>
<tr><td rowspan="6">3:2</td><td rowspan="6">AGC_FREEZE[1:0]</td><td rowspan="6">0 (00)</td><td rowspan="6">R/W</td><td colspan="3">Control when the AGC gain should be frozen.</td></tr>
<tr><td>Setting</td><td colspan="2">Function</td></tr>
<tr><td>0 (00)</td><td colspan="2">Normal operation. Always adjust gain when required.</td></tr>
<tr><td>1 (01)</td><td colspan="2">The gain setting is frozen when a sync word has been found.</td></tr>
<tr><td>2 (10)</td><td colspan="2">Manually freeze the analogue gain setting and continue to adjust the digital gain.</td></tr>
<tr><td>3 (11)</td><td colspan="2">Manually freezes both the analogue and the digital gain setting. Used for manually overriding the gain.</td></tr>
<tr><td rowspan="6">1:0</td><td rowspan="6">FILTER_LENGTH[1:0]</td><td rowspan="6">1 (01)</td><td rowspan="6">R/W</td><td colspan="3">2-FSK and 4-FSK: Sets the averaging length for the amplitude from the channel filter.
OOK: Sets the OOK decision boundary for OOK reception.</td></tr>
<tr><td>Setting</td><td>Channel filter samples</td><td>OOK decision boundary</td></tr>
<tr><td>0 (00)</td><td>8</td><td>4 dB</td></tr>
<tr><td>1 (01)</td><td>16</td><td>8 dB</td></tr>
<tr><td>2 (10)</td><td>32</td><td>12 dB</td></tr>
<tr><td>3 (11)</td><td>64</td><td>16 dB</td></tr>
</table>

0x20: RESERVED

Bit	Field Name	Reset	R/W	Description
7:3		31 (11111)	R/W	Use setting from SmartRF Studio [4]
2			R0	Not used
1:0		0 (00)	R/W	Use setting from SmartRF Studio [4]

0x21: FREND1 - Front End RX Configuration

Bit	Field Name	Reset	R/W	Description
7:6	LNA_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end LNA PTAT current output
5:4	LNA2MIX_CURRENT[1:0]	1 (01)	R/W	Adjusts front-end PTAT outputs
3:2	LODIV_BUF_CURRENT_RX[1:0]	1 (01)	R/W	Adjusts current in RX LO buffer (LO input to mixer)
1:0	MIX_CURRENT[1:0]	2 (10)	R/W	Adjusts current in mixer

0x22: FREND0 - Front End TX Configuration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5:4	LODIV_BUF_CURRENT_TX[1:0]	1 (01)	R/W	Adjusts current TX LO buffer (input to PA). The value to use in this field is given by the SmartRF Studio software [4].
3			R0	Not used
2:0	PA_POWER[2:0]	0 (000)	R/W	Selects PA power setting. This value is an index to the PATABLE, which can be programmed with up to 2 different PA settings. When using OOK, PA_POWER should be 001, and for all other modulation formats it should be 000. Please see Sections 10.6 and Section 23 more details.

FSCAL3 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6	FSCAL3[7:6]	2 (10)	R/W	Frequency synthesizer calibration configuration. The value to write in this field before calibration is given by the SmartRF Studio software [4].
5:4	CHP_CURR_CAL_EN[1:0]	2 (10)	R/W	Disable charge pump calibration stage when 0.
3:0	FSCAL3[3:0]	9 (1001)	R/W	Frequency synthesizer calibration result register. Digital bit vector defining the charge pump output current, on an exponential scale: $I\_OUT = I_0 \cdot 2^{FSCAL3[3:0]/4}$ Please see Section 26.2 for more details.

0x24: FSCAL2 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5	VCO_CORE_H_EN	0	R/W	Choose high (1) / low (0) VCO
4:0	FSCAL2[4:0]	10 (01010)	R/W	Frequency synthesizer calibration result register. VCO current calibration result and override value. Please see Section 26.2 for more details.

0x25: FSCAL1 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7:6			R0	Not used
5:0	FSCAL1[5:0]	32 (0x20)	R/W	Frequency synthesizer calibration result register. Capacitor array setting for VCO coarse tuning. Please see Section 26.2 for more details.

0x26: FSCAL0 - Frequency Synthesizer Calibration

Bit	Field Name	Reset	R/W	Description
7			R0	Not used
6:0	FSCAL0[6:0]	13 (0x0D)	R/W	Frequency synthesizer calibration control. The value to use in this register is given by the SmartRF Studio software [4]

27.2 Configuration Register Details - Registers that Loose Programming in SLEEP State

0x29: RESERVED

Bit	Field Name	Reset	R/W	Description
7:0		89 (0x59)	R/W	Use setting from SmartRF Studio [4]

0x2A: RESERVED

Bit	Field Name	Reset	R/W	Description
7:0		127 (0x7F)	R/W	Use setting from SmartRF Studio [4]

0x2B: RESERVED

Bit	Field Name	Reset	R/W	Description
7:0		63 (0x3F)	R/W	Use setting from SmartRF Studio [4]

0x2C: TEST2 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST2[7:0]	136 (0x88)	R/W	Use setting from SmartRF Studio [4] This register will be forced to 0x88 or 0x81 when it wakes up from SLEEP mode, depending on the configuration of `FIFOTHR.ADC_RETENTION`. Note that the value read from this register when waking up from SLEEP always is the reset value (0x88) regardless of the `ADC_RETENTION` setting. The inverting of some of the bits due to the `ADC_RETENTION` setting is only seen INTERNALLY in the analog part.

0x2D: TEST1 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:0	TEST1[7:0]	49 (0x31)	R/W	Use setting from SmartRF Studio [4] This register will be forced to 0x31 or 0x35 when it wakes up from SLEEP mode, depending on the configuration of `FIFOTHR.ADC_RETENTION`. Note that the value read from this register when waking up from SLEEP always is the reset value (0x31) regardless of the `ADC_RETENTION` setting. The inverting of some of the bits due to the `ADC_RETENTION` setting is only seen INTERNALLY in the analog part.

0x2E: TEST0 - Various Test Settings

Bit	Field Name	Reset	R/W	Description
7:2	TEST0[7:2]	2 (000010)	R/W	Use setting from SmartRF Studio [4]
1	VCO_SEL_CAL_EN	1	R/W	Enable VCO selection calibration stage when 1
0	TEST0[0]	1	R/W	Use setting from SmartRF Studio [4]

27.3 Status Register Details

0x30 (0xF0): PARTNUM - Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	PARTNUM[7:0]	0 (0x00)	R	Chip part number

0x31 (0xF1): VERSION - Chip ID

Bit	Field Name	Reset	R/W	Description
7:0	VERSION[7:0]	7 (0x07)	R	Chip version number.

0x32 (0xF2): FREQEST - Frequency Offset Estimate from Demodulator

Bit	Field Name	Reset	R/W	Description
7:0	FREQOFF_EST		R	The estimated frequency offset (2's complement) of the carrier. Resolution is $F_{XTAL}/2^{14}$ (1.59 - 1.65 kHz); range is ±202 kHz to ±210 kHz, depending on XTAL frequency. Frequency offset compensation is only supported for 2-FSK, GFSK, and 4-FSK modulation. This register will read 0 when using OOK modulation.

0x33 (0xF3): CRC_REG - CRC OK

Bit	Field Name	Reset	R/W	Description
7	CRC OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6:0			R	Reserved

0x34 (0xF4): RSSI - Received Signal Strength Indication

Bit	Field Name	Reset	R/W	Description
7:0	RSSI		R	Received signal strength indicator

0x35 (0xF5): MARCSTATE - Main Radio Control State Machine State

<table>
<tr><th>Bit</th><th>Field Name</th><th>Reset</th><th>R/W</th><th colspan="3">Description</th></tr>
<tr><td>7:5</td><td></td><td></td><td>R0</td><td colspan="3">Not used</td></tr>
<tr><td rowspan="26">4:0</td><td rowspan="26">MARC_STATE[4:0]</td><td rowspan="26"></td><td rowspan="26">R</td><td colspan="3">Main Radio Control FSM State</td></tr>
<tr><td>Value</td><td>State name</td><td>State (Figure 19, page 39)</td></tr>
<tr><td>0 (0x00)</td><td>SLEEP</td><td>SLEEP</td></tr>
<tr><td>1 (0x01)</td><td>IDLE</td><td>IDLE</td></tr>
<tr><td>2 (0x02)</td><td>XOFF</td><td>XOFF</td></tr>
<tr><td>3 (0x03)</td><td>VCOON_MC</td><td>MANCAL</td></tr>
<tr><td>4 (0x04)</td><td>REGON_MC</td><td>MANCAL</td></tr>
<tr><td>5 (0x05)</td><td>MANCAL</td><td>MANCAL</td></tr>
<tr><td>6 (0x06)</td><td>VCOON</td><td>FS_WAKEUP</td></tr>
<tr><td>7 (0x07)</td><td>REGON</td><td>FS_WAKEUP</td></tr>
<tr><td>8 (0x08)</td><td>STARTCAL</td><td>CALIBRATE</td></tr>
<tr><td>9 (0x09)</td><td>BWBOOST</td><td>SETTLING</td></tr>
<tr><td>10 (0x0A)</td><td>FS_LOCK</td><td>SETTLING</td></tr>
<tr><td>11 (0x0B)</td><td>IFADCON</td><td>SETTLING</td></tr>
<tr><td>12 (0x0C)</td><td>ENDCAL</td><td>CALIBRATE</td></tr>
<tr><td>13 (0x0D)</td><td>RX</td><td>RX</td></tr>
<tr><td>14 (0x0E)</td><td>RX_END</td><td>RX</td></tr>
<tr><td>15 (0x0F)</td><td>RX_RST</td><td>RX</td></tr>
<tr><td>16 (0x10)</td><td>TXRX_SWITCH</td><td>TXRX_SETTLING</td></tr>
<tr><td>17 (0x11)</td><td>RXFIFO_OVERFLOW</td><td>RXFIFO_OVERFLOW</td></tr>
<tr><td>17 (0x11)</td><td>RXFIFO_OVERFLOW</td><td>RXFIFO_OVERFLOW</td></tr>
<tr><td>18 (0x12)</td><td>FSTXON</td><td>FSTXON</td></tr>
<tr><td>19 (0x13)</td><td>TX</td><td>TX</td></tr>
<tr><td>20 (0x14)</td><td>TX_END</td><td>TX</td></tr>
<tr><td>21 (0x15)</td><td>RXTX_SWITCH</td><td>RXTX_SETTLING</td></tr>
<tr><td>22 (0x16)</td><td>TXFIFO_UNDERFLOW</td><td>TXFIFO_UNDERFLOW</td></tr>
<tr><td colspan="3">Note: it is not possible to read back the SLEEP or XOFF state numbers because setting CSn low will make the chip enter the IDLE mode from the SLEEP or XOFF states.</td></tr>
</table>

0x38 (0xF8): PKTSTATUS - Current GDOx Status and Packet Status

Bit	Field Name	Reset	R/W	Description
7	CRC_OK		R	The last CRC comparison matched. Cleared when entering/restarting RX mode.
6	CS		R	Carrier sense. Cleared when entering IDLE mode.
5				Reserved
4	CCA		R	Channel is clear
3	SFD		R	Start of Frame Delimiter. This bit is asserted when sync word has been received and de-asserted at the end of the packet. It will also de-assert when a packet is discarded due to address or maximum length filtering or the radio enters RXFIFO_OVERFLOW state.
2	GDO2		R	Current GDO2 value. Note: the reading gives the non-inverted value irrespective of what `IOCFG2.GDO2_INV` is programmed to. It is not recommended to check for PLL lock by reading `PKTSTATUS[2]` with `GDO2_CFG=0x0A`.
1			R0	Not used
0	GDO0		R	Current GDO0 value. Note: the reading gives the non-inverted value irrespective of what `IOCFG0.GDO0_INV` is programmed to. It is not recommended to check for PLL lock by reading `PKTSTATUS[0]` with `GDO0_CFG=0x0A`.

0x3A (0xFA): TXBYTES - Underflow and Number of Bytes

Bit	Field Name	Reset	R/W	Description
7	TXFIFO_UNDERFLOW		R	
6:0	NUM_TXBYTES		R	Number of bytes in TX FIFO

0x3B (0xFB): RXBYTES - Overflow and Number of Bytes

Bit	Field Name	Reset	R/W	Description
7	RXFIFO_OVERFLOW		R	
6:0	NUM_RXBYTES		R	Number of bytes in RX FIFO

28 Development Kit Ordering Information

Orderable Evaluation Module	Description	Minimum Order Quantity
CC11xLDK-868-915	CC11xL Development Kit, 868/915 MHz	1
CC11xLEMK-433	CC11xL Evaluation Module Kit, 433 MHz	1
RF BoosterPack for MSP430 LaunchPad	Plug-in boards for the MSP430 Value Line LaunchPad (MSP-EXP430G2), 868/915 MHz	1

Figure 25: Development Kit Ordering Information

29 References

[1] Characterization Design 315 - 433 MHz

(Identical to the CC1101EM 315 - 433 MHz Reference Design (swrr046.zip))

[2] Characterization Design 868 - 915 MHz

(Identical to the CC1101EM 868 - 915 MHz Reference Design (swrr045.zip))

[3] CC110L Errata Notes (swrz037.pdf)

[4] SmartRF Studio (swrc176.zip)

[5] DN010 Close-in Reception with CC1101 (swra147.pdf)

[6] DN017 CC11xx 868/915 MHz RF Matching (swra168.pdf)

[7] DN015 Permanent Frequency Offset Compensation (swra159.pdf)

[8] DN006 CC11xx Settings for FCC 15.247 Solutions (swra123.pdf)

[9] DN505 RSSI Interpretation and Timing (swra114.pdf)

[10] DN013 Programming Output Power on CC1101 (swra168.pdf)

[11] DN022 CC11xx OOK/ASK register settings (swra215.pdf)

[12] DN005 CC11xx Sensitivity versus Frequency Offset and Crystal Accuracy (swra122.pdf)

[13] CC1190 Data Sheet (swrs089.pdf)

[14] AN094 Using the CC1190 Front End with CC1101 under EN 300 220 (swra356.pdf)

[15] AN096 Using the CC1190 Front End with CC1101 under FCC 15.247 (swra361.pdf)

[16] DN032 Options for Cost Optimized CC11xx Matching (swra346.pdf)

[17] CC110LEM / CC115LEM 433 MHz Reference Design (swrr081.zip)

[18] CC110LEM / CC115LEM 868 - 915 MHz Reference Design (swrr082.zip)

30 General Information

30.1 Document History

Revision	Date	Description/Changes
SWRS109	05.24.2011	Initial Release
SWRS109A	08.09.2011	Added two registers (CHANNR and MDMCFG0) in addition to the MDMCFG1.CHANSPC_E register field. Changes made to Section 20. Hyperlinks added to the CC110LEM / CC115LEM 433 MHz Reference Design and the CC110LEM / CC115LEM 868 - 915 MHz Reference Design

Table 41: Document History

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CC110LRGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC110L	Samples
CC110LRGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	CC110L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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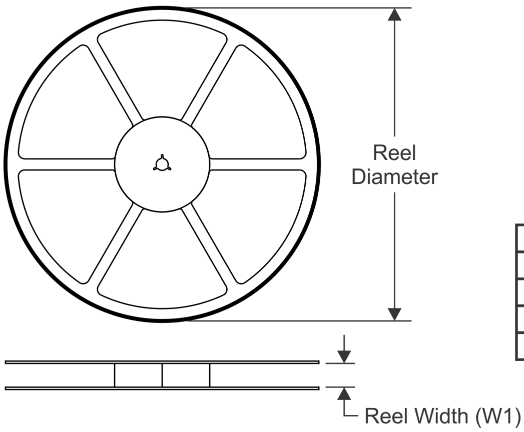
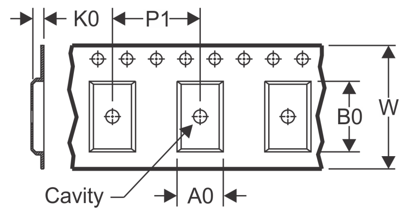
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

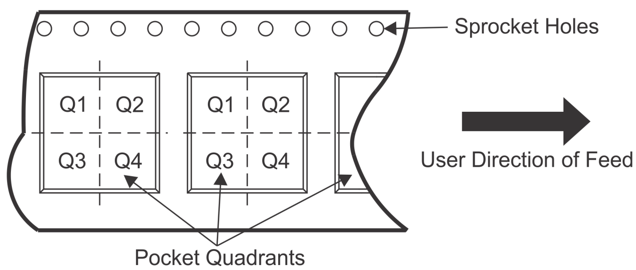
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

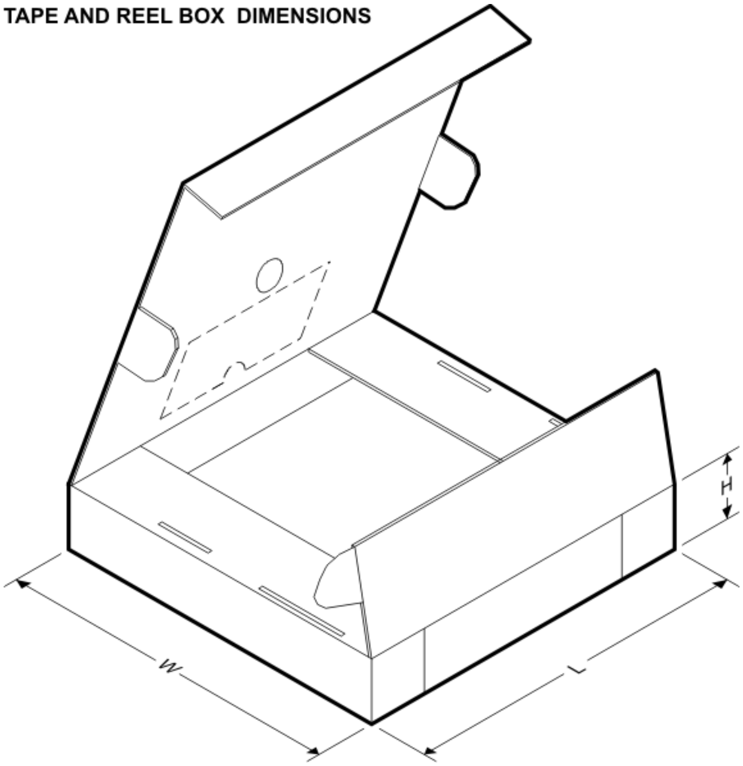
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CC110LRGPR	QFN	RGP	20	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
CC110LRGPT	QFN	RGP	20	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

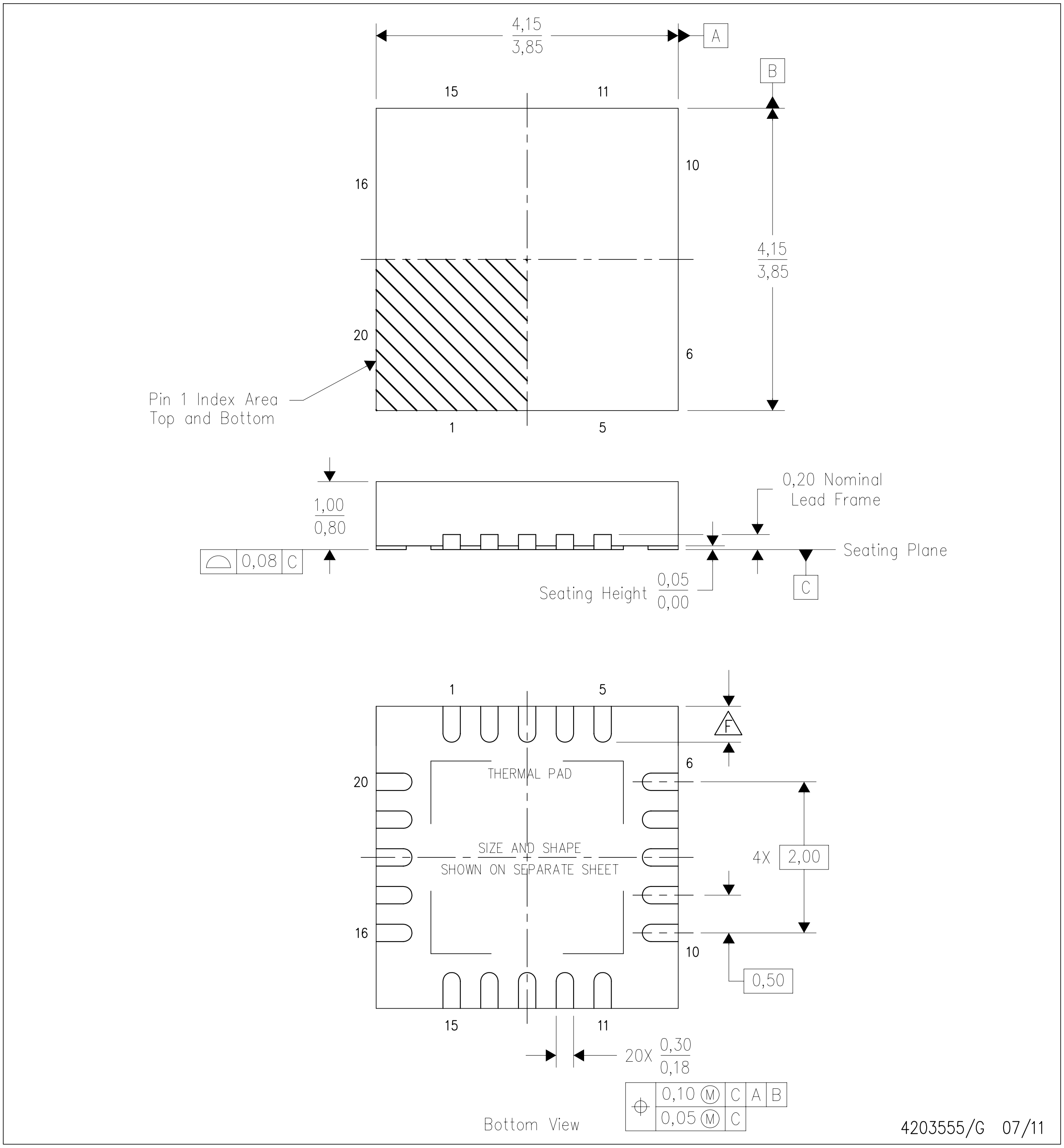
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CC110LRGPR	QFN	RGP	20	3000	338.1	338.1	20.6
CC110LRGPT	QFN	RGP	20	250	338.1	338.1	20.6

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

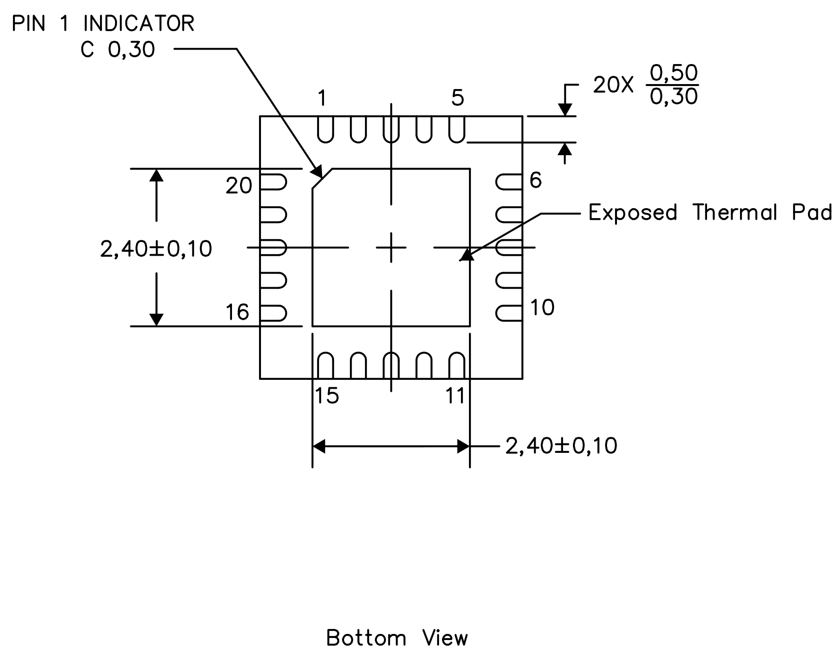
RGP (S-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206346-7/Y 12/12

NOTES: A. All linear dimensions are in millimeters