ERRATA NOTE

CC1110Fx/CC1111Fx

Table Of Contents

1 Part May Hang in Power Mode

The following applies only to power mode 2 and 3.

1.1 Description of the Problem

When waking up from power mode 2 and 3 there is a small chance that the `SLEEP.MODE` bits are faulty set to a value other than zero before the `PCON.IDLE` bit is cleared by the CPU. This causes the chip to re-enter power mode immediately. Since an enabled interrupt is pending at this point, the chip will wake up and re-enter power mode continuously and appear to hang.

Once the device hang, only a system reset will get the chip back to normal operation.

1.2 Suggested Work-around

By ensuring that the `SLEEP.MODE` bits are written to zero at the instant the chip wakes from power mode, the chip will never re-enter power mode unintentionally.

If the following conditions are met, this can be done by setting up a DMA transfer to the `SLEEP` register that is triggered right before writing the `PCON.IDLE` bit.

- The chip is running at the HS RC oscillator at the highest possible clock speed setting
- The high speed crystal oscillator is powered down
- Flash Cache is disabled

Please note that the requirements stated in the following chapters of the data sheet still applies: *Power Management Control* and *Sleep Timer and Power Modes*.

Note: The following code assumes the chip is already running at the HS RC oscillator with the highest clock speed setting possible and this has to be handled by the application. The code marked blue below is timing critical and should be done in the order as shown here with no intervening code.

```
// Initialization of source buffers and DMA descriptor for the DMA transfer
unsigned char __xdata PM2_BUF[7] = {0x06,0x06,0x06,0x06,0x06,0x06,0x04};
unsigned char __xdata PM3_BUF[7] = {0x07,0x07,0x07,0x07,0x07,0x07,0x04};
unsigned char __xdata dmaDesc[8] = {0x00,0x00,0xDF,0xBE,0x00,0x07,0x20,0x42};

// Store current DMA channel 0 descriptor and abort any ongoing transfers if
// the channel is in use
unsigned char storedDescHigh = DMA0CFGH;
unsigned char storedDescLow = DMA0CFGL;
DMAARM |= 0x81;

// Update descriptor with correct source
// NB! Replace &PM2_BUF with &PM3_BUF if powermode 3 is chosen instead
dmaDesc[0] = (unsigned int)& PM2_BUF >> 8;
dmaDesc[1] = (unsigned int)& PM2_BUF;

// Associate the descriptor with DMA channel 0 and arm the DMA channel
DMA0CFGH = (unsigned int)&dmaDesc >> 8;
DMA0CFGL = (unsigned int)&dmaDesc;
DMAARM = 0x01;

// NOTE! At this point, make sure all interrupts that will not be used to
// wake from PM are disabled as described in chapter 13.1.3 of the datasheet.

// Align with positive 32 kHz clock edge as described in chapter 13.8.2
// of the datasheet.
char temp = WORTIME0;
while( temp == WORTIME0);

// Make sure XOSC is powered down when entering PM2/3 and that the flash
// cache is disabled
// NB! Replace 0x06 with 0x07 if power mode 3 is chosen instead
MEMCTR |= 0x02;
SLEEP = 0x06;

// Enter power mode as described in chapter 13.1.3 in the datasheet.
// Make sure DMA channel 0 is triggered just before setting PCON.IDLE
asm("NOP");
asm("NOP");
asm("NOP");
if( SLEEP & 0x03 ) {
    asm(“MOV 0xD7,#0x01”);     // DMAREQ = 0x01;
    asm(“NOP”);                // Needed to perfectly align the DMA transfer
    asm(“ORL 0x87,#0x01”);     // PCON |= 0x01;
    asm("NOP");
}

// Enable Flash Cache
MEMCTR &= ~0x02;

// Update DMA channel 0 with original descriptor and arm channel if it was in
// use before PM was entered
DMA0CFGH = storedDescHigh;
DMA0CFGL = storedDescLow;
DMAARM = 0x01;
```

2 RX_OVERFLOW Issue

2.1 Description of the Problem

In addition to the RFD register, the *CC1110Fx/CC1111Fx* has several internal buffers for status registers, CRC bytes, and buffers used when FEC is enabled. If there is a byte in the RFD register and more bytes are written to this register by the radio, the radio will enter RX_OVERFLOW state. There are however some cases where the radio will be stuck in RX state instead of entering RX_OVERFLOW state, as it should. Below is a table showing the register settings that will cause this problem. APPEND_STATUS is found in the PKTCTRL1 register, CRC_EN is found in the PKTCTRL0 register, and FEC_EN is in the MDMCFG1 register. In the table below, x is the number of bytes that will be written to the RFD register by the radio (including the status bytes if APPEND_STATUS = 1). Assume that the radio is configured to enter IDLE state after a packet has been received.

When the radio is stuck in RX state like this, it will draw current as in RX state, but it will not be able to receive any more data. Neither RFIF.IRQ_DONE nor RFIF.IRQ_RX_OVF will be asserted. The only way to proceed is by issuing an SIDLE strobe command (RFST = 0x04).

Register Settings	# of Bytes Read from the RFD Register	MARCSTATE	Comment

APPEND_STATUS = 1
CRC_EN = 0
FEC_EN = 0
	x − 1	RX_OVERFLOW	Ok

	x	IDLE	Ok

APPEND_STATUS = 1
CRC_EN = 0
FEC_EN = 1
	x − 6	RX_OVERFLOW	Ok

	x − 5	RX	Not ok. Stuck in RX
	x − 4	RX	Not ok. Stuck in RX
	x − 3	RX	Not ok. Stuck in RX
	x − 2	RX	Not ok. Stuck in RX
	x − 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok

APPEND_STATUS = 1
CRC_EN = 1
FEC_EN = 0
	x − 3	RX_OVERFLOW	Ok

	x − 2	RX	Not ok. Stuck in RX
	x − 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok

APPEND_STATUS = 1
CRC_EN = 1
FEC_EN = 1
	x − 5	RX_OVERFLOW	Ok

	x − 4	RX	Not ok. Stuck in RX
	x − 3	RX	Not ok. Stuck in RX
	x − 2	RX	Not ok. Stuck in RX
	x − 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok

APPEND_STATUS = 0
CRC_EN = 0
FEC_EN = 0
	x − 1	RX_OVERFLOW	Ok

	x	IDLE	Ok

APPEND_STATUS = 0
CRC_EN = 0
FEC_EN = 1
	x − 4	RX_OVERFLOW	Ok

	x − 3	RX	Not ok. Stuck in RX
	x − 2	RX	Not ok. Stuck in RX
	x − 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok

APPEND_STATUS = 0
CRC_EN = 1
FEC_EN = 0
	x − 1	RX_OVERFLOW	Ok

	x	IDLE	Ok

APPEND_STATUS = 0
CRC_EN = 1
FEC_EN = 1
	x − 3	RX_OVERFLOW	Ok

	x − 2	RX	Not ok. Stuck in RX
	x − 1	RX	Not ok. Stuck in RX
	x	IDLE	Ok

2.2 Suggested Work-around

In applications where the DMA is used to read the RFD register, it is important to configure the DMA in accordance with the chosen radio configuration. Please see DN107 for more details on how this should be done. If the RFD register is read manually, it is important that the register is read when the RFTXRXIF flag in the TCON register has been asserted. If the RFTXRX interrupt is used, it is important that this interrupt has a high priority. If a polling scheme is used, one needs to make sure that interrupts that are enabled will not prevent the RFD register to be read before a new byte is received.

3 Document History

Revision	Date	Description/Changes
SWRZ022B	2007-12-21	Updated with issue related to RX_OVERFLOW state. Removed "Batches Affected" since there is only one revision available of this product.
SWRZ022A	2007-09-18	Updated with clarified conditions for the fix and update the code to remove instability.
SWRZ022	2007-09-06	Released for RTM

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