

RSSI Interpretation and Timing

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Keywords

- CC430
- CC1100
- CC1100E
- CC1101
- CC1110
- CC1111
- CC2500
- CC2510
- CC2511
- RSSI

1 Introduction

The Received Signal Strength Indicator (RSSI) is a measure of the RF power input to the transceiver. The RSSI value is based on the gain setting in the RX chain and the measured signal level in the channel. In RX mode, the RSSI value can be read continuously from the `RSSI` status

register until the demodulator detects a sync word (when sync word detection is enabled). At that point the RSSI readout value is frozen until the next time the chip enters RX mode. If sync word detection is disabled, the `RSSI` register will be continuously updated.

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2 Abbreviations

AGC	Automatic Gain Control
BW	Band Width
CS	Carrier Sense
N/A	Not available
RX	Receive mode
RSSI	Received Signal Strength Indicator
WOR	Wake on Radio

3 RSSI Register Interpretation

The RSSI value read from the `RSSI` status register is a 2's complement number and is in dBm with ½ dB resolution. The following procedure can be used to convert the RSSI reading to an absolute power level (`RSSI_dBm`).

Assume that the RSSI offset is 72 dB and that `11111010b` is read from the `RSSI` register.

If `11111010b` is interpreted as a 2's complement number it has the value -6.

This means that the RSSI value, before taking the offset into account, is -3 dBm. Subtracting the RSSI offset, the RSSI value in dBm ends up at -3 dBm - 72 dB = -75 dBm.

```

UINT8 rssi_dec;
INT16 rssi_dBm;
UINT8 rssi_offset = 72;

rssi_dec = halSpiReadStatus(CCxxx0_RSSI);

if (rssi_dec >= 128)
    rssi_dBm = (INT16)((INT16)( rssi_dec - 256) / 2) - rssi_offset;
else
    rssi_dBm = (rssi_dec / 2) - rssi_offset;
    
```

Note that the code will be slightly different for SoC's as the register is not accessed over the SPI interface.

4 RSSI Offset

The RSSI offset will vary with register settings. Different data rates will therefore have different RSSI offsets. Table 1 shows the RSSI offset for some data rates for CC430, CC1100, CC1100E, CC1101, CC1110/CC1111, CC2500, and CC2510/CC2511.

Data Rate [kBaud]	CC1100		CC1101		CC1110/CC1111		
	RSSI Offset [dB]		RSSI Offset [dB]		RSSI Offset [dB]		
	433 [MHz]	868 [MHz]	433 [MHz]	868 [MHz]	315 [MHz]	433 [MHz]	868 [MHz]
1.2	75	74	74	74	74	75	73
38.4	75	74	74	74	73	74	73
250	79	78	74	74	74	73	77
500	79	77	74	74	-	-	-

Data Rate [kBaud]	CC430		CC1100E		CC2500	CC2510/CC2511
	RSSI Offset [dB]		RSSI Offset [dB]		RSSI Offset [dB]	RSSI Offset [dB]
	433 [MHz]	868 [MHz]	490 [MHz]	955 [MHz]		
1.2	74	74	75	75	-	-
2.4	-	-	-	-	71	74
10	-	-	-	-	69	74
38.4	74	74	75	75	-	-
250	74	74	N/A	79	72	71
500	74	74	79	N/A	72	72

Table 1. RSSI Offset

When using data rates other than the ones in Table 1 it is possible to find the RSSI offset by applying a known input power and then read out the RSSI value.

5 RSSI Response Time

The following sections provide background on how the AGC works and when to expect RSSI updates. Equations that predict the RSSI response time will be compared to measurements at the end of this section.

5.1 AGC Background

The main purpose of the AGC module is to adjust the gain of the analogue LNAs and the digital VGA, so that the IF-ADC and DVGA are not saturated and the demodulator is able to perform demodulation. The module also reports the received signal level (RSSI), and indicates if a carrier is present (carrier sense).

The AGC module is basically part of a control loop, which aims to keep the in-band signal level in the demodulator constant, regardless of the signal level at the antenna. The AGC module low-pass filters the magnitude signal and compares the value to a programmable target magnitude (`AGCCTRL2.MAGN_TARGET`). The new gain setting is calculated by adding the deviation from the target magnitude to the previous gain setting.

The low-pass filter is an accumulate-and-dump filter with programmable length (`AGCCTRL0.FILTER_LENGTH`). To avoid frequent AGC gain-switching activity (e.g. for noisy signals) it might be an idea to increase the filter length. The AGC module has a configurable wait time after each gain adjustment (`AGCCTRL0.WAIT_TIME`) to stabilize the control loop. The AGC will ignore all samples in the wait time, and thereby give the effects of the gain change a chance to propagate through the analogue mixer and the demodulator. The wait time might be too short if the AGC module exhibits stability problems (e.g. large overshoot when adjusting the gain).

5.2 RSSI Response Time

Figure 1 shows an example of how the RSSI value is updated after the chip is put in RX. It takes a finite time, T_0 , for signals to propagate through the demodulator when the chip is put in RX. The intervals $T_{1,n}$ and T_2 are AGC specific.

- $T_{1,n}$ represents the time the AGC waits after performing a gain change.
- T_2 represents the time the AGC uses to average the magnitude samples from the demodulator.

An update of the RSSI value occurs at the end of each T_2 interval. The RSSI value is not valid before the AGC settling phase is finished, indicated by RSSI#4 in Figure 1. After this instant the gain will not likely be further altered and each update of the RSSI value can be considered as valid. The duration from entering RX to the first valid RSSI update is denoted RSSI response time.

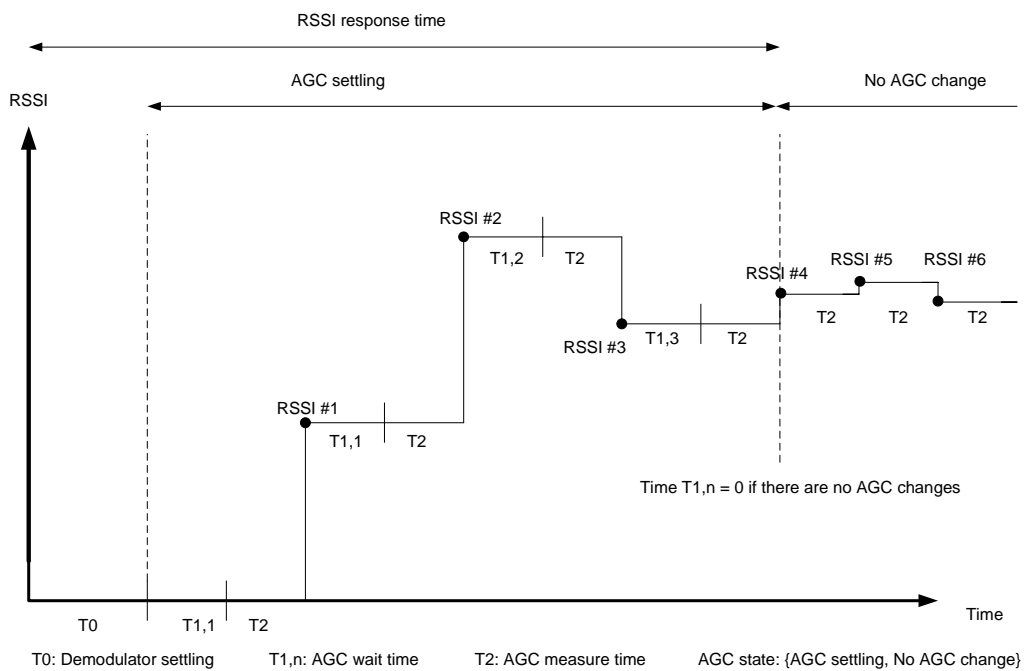


Figure 1. RSSI Response Time

In Figure 1 we see that the RSSI register update rate varies after entering RX mode depending on the AGC state ("AGC settling" or "No AGC change"). The figure does, however, not show how the input power effects the time spent in the AGC settling state. Generally, a stronger input signal can lead to a longer AGC settling phase than a weaker input signal since multiple gain changes are more likely to occur. This fact complicates applications where one wants to spend a minimum pre-determined time in RX before reading the RSSI register since received power has a stochastic nature. In such cases one should do a set of measurements where a known strong signal is input to the receiver and the RSSI register is read continuously. One should then measure the time from the radio enters RX state until a valid RSSI value is available. This time value will be the maximum time value of the RSSI response time. Figure 2, Figure 3, and Figure 4 shows 3 different signals strengths (-50 dBm, -70 dBm, and -86 dBm) at 3 different data rates (2.4 kBaud, 10 kBaud, and 250 kBaud) and the corresponding RSSI response time. CC2500 was used for this test and register settings were obtained from SmartRF[®] Studio.

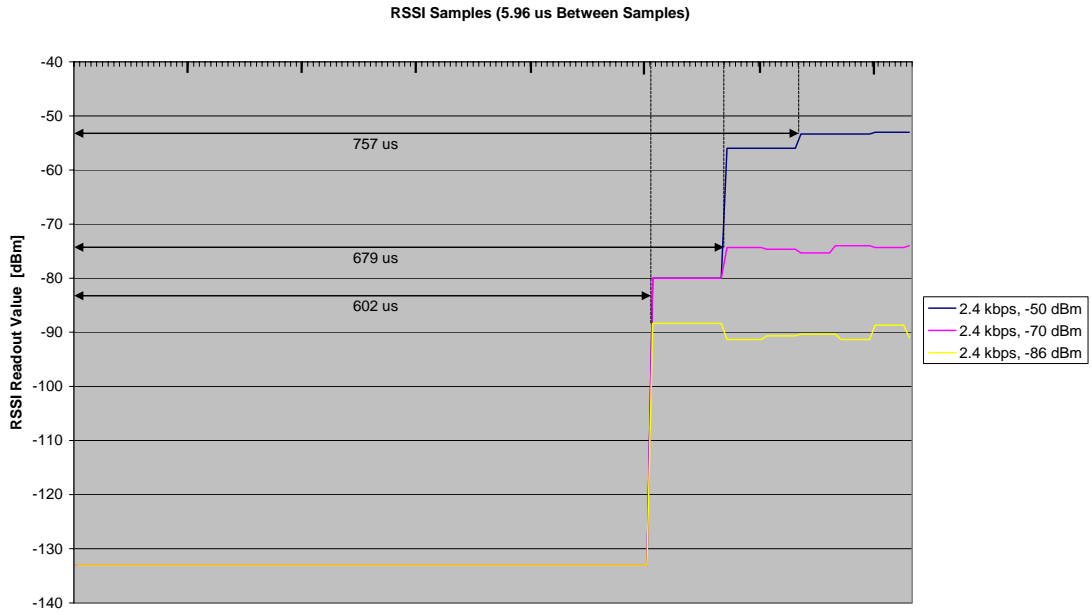


Figure 2. RSSI Value vs. Time (2.4 kBaud)

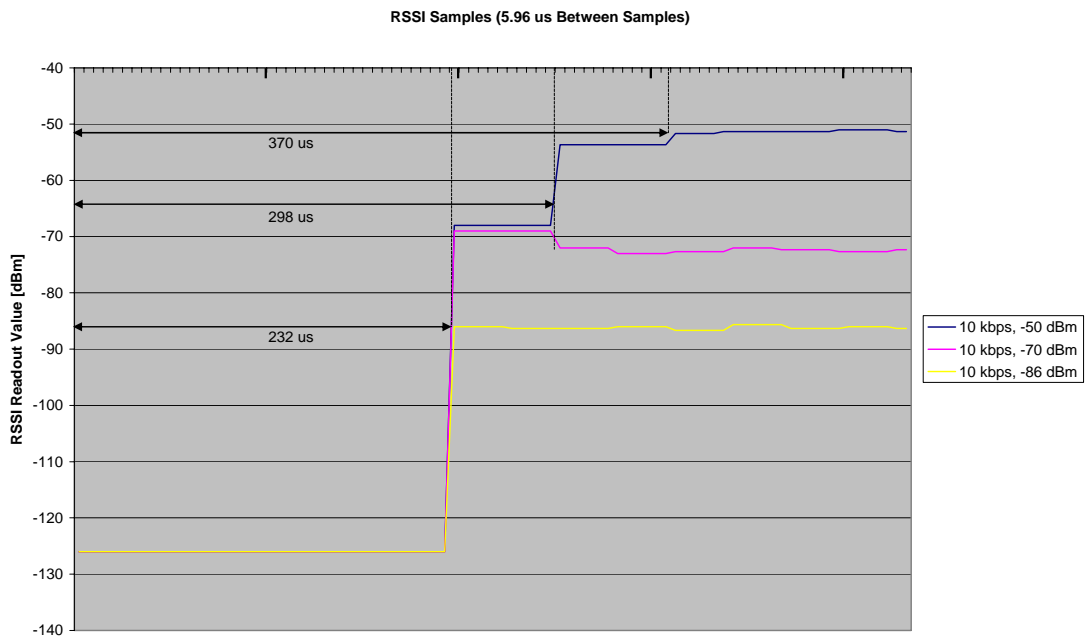


Figure 3. RSSI Value vs. Time (10 kBaud)

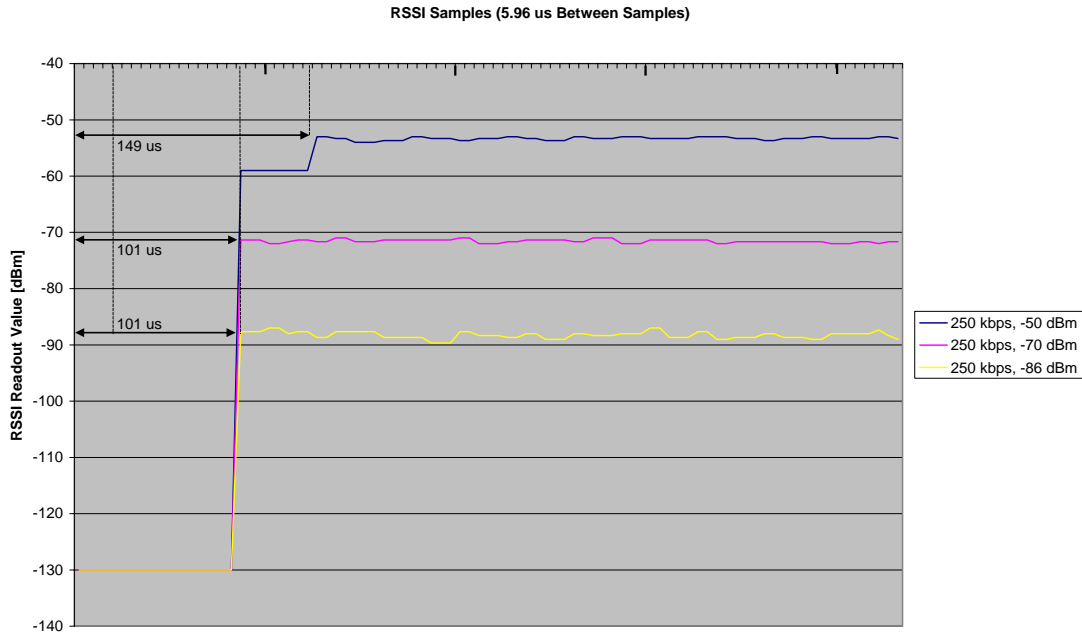


Figure 4. RSSI Value vs. Time (250 kBaud)

Pseudo-code for test firmware:

1. Strobe RX
2. Wait until the radio is in RX mode
3. Start reading the `RSSI` register repeatedly and store the values in a buffer (for the plots in Figure 2 , Figure 3, and Figure 4, the `RSSI` register was read 250 times, with 5.96 us between readings). It can also be convenient to use timers and interrupts for this test depending on chip type.
4. From the `RSSI` register values, calculate the actual RSSI value and plot the RSSI values vs. time.

The following sections provide equations for the T_0 , $T_{1,n}$ and T_2 intervals in Figure 1. These equations can be used to estimate the time `RSSI#1` occurs with very high resolution. The RSSI response time can therefore be quite accurately estimated for low signal strengths. The equations also facilitate the calculation of maximum subsequent RSSI update instants, and provide the worst case RSSI response time given an arbitrary number of gain changes..

The equations for estimating the RSSI response time can for example be used when estimating the time the radio will be in RX when using WOR and direct RX termination based on RSSI measurements (`MCSM2.RX_TIME_RSSI = 1`). Using this feature, RX mode will be terminated if the RSSI level is below a programmable threshold.

5.2.1 Calculation of Receiver Bandwidth and Data Rate

The receiver filter bandwidth ($BW_{channel}$) and data rate (R_{DATA}) depend on crystal frequency (f_{XOSC}) and the configuration of `MDMCFG4` and `MDMCFG3` registers:

$$BW_{channel} = \frac{f_{XOSC}}{8 \cdot (4 + CHANBW_M) \cdot 2^{CHANBW_E}}$$

Equation 1. Receiver Filter Bandwidth

$$R_{DATA} = \frac{(256 + DRATE_M) \cdot 2^{DRATE_E}}{2^{28}} \cdot f_{XOSC}$$

Equation 2. Data Rate

5.2.2 Calculation of T_0

The value of T_0 depends on receiver filter bandwidth, data rate, and register MDMCFG2.DEM_DCFILT_OFF, which is 0 for sensitivity optimized reception and 1 for current optimized reception.

$$T_0 = MAX \left\{ \frac{\text{ceiling} \left[\frac{1023 \cdot 2 \cdot BW_{channel}}{f_{XOSC}} ; 1 \right] + 19}{2 \cdot BW_{channel}} + \frac{2.5}{f_{XOSC}} ; \frac{\text{ceiling} \left[\frac{1022 \cdot 8 \cdot R_{DATA}}{f_{XOSC}} ; 1 \right] + 9}{8 \cdot R_{DATA}} + \frac{4.5}{f_{XOSC}} \right\}$$

Equation 3. T_0 when MDMCFG2.DEM_DCFILT_OFF = 0

The ceiling(X; 1) - function rounds X upwards to closest integer.

$$T_0 = MAX \left\{ \frac{10}{BW_{channel}} + \frac{2.5}{f_{XOSC}} ; \frac{10}{8 \cdot R_{DATA}} + \frac{4.5}{f_{XOSC}} \right\}$$

Equation 4. T_0 when MDMCFG2.DEM_DCFILT_OFF = 1

5.2.3 Calculation of $T_{1,n}$

The value of interval $T_{1,1}$ can be found exactly for modulation formats not equal to OOK/ASK, i.e. MDMCFG2.MOD_FORMAT != 3. For OOK/ASK a *maximum* value is provided. The WAIT_TIME value is located in the AGCTRL0 register.

$$T_{1,1} = \frac{8 \cdot WAIT_TIME + 7 + \text{ceiling} \left[2 \cdot \left(T_0 - \frac{1.5}{f_{XOSC}} \right) \cdot BW_{channel} ; 1 \right]}{2 \cdot BW_{channel}} - T_0 + \frac{2.5}{f_{XOSC}}$$

$$T_{1,n} \leq \frac{8 \cdot (WAIT_TIME + 1)}{2 \cdot BW_{channel}} + \frac{1}{f_{XOSC}}, n = \{2, 3, 4, \dots\}$$

Equation 5. $T_{1,n}$ when MDMCFG2.MOD_FORMAT != ASK/OOK

$$T_{1,1} \leq \frac{8 \cdot \text{WAIT_TIME} + 6 + \text{ceiling} \left[2 \cdot \left(T_0 - \frac{1.5}{f_{XOSC}} \right) \cdot BW_{\text{channel}}; 1 \right]}{2 \cdot BW_{\text{channel}}} - T_0 + \frac{2.5}{f_{XOSC}} + \frac{1}{8 \cdot R_{\text{DATA}}}$$

$$T_{1,n} \leq \frac{8 \cdot \text{WAIT_TIME} + 7}{2 \cdot BW_{\text{channel}}} + \frac{1}{f_{XOSC}} + \frac{1}{8 \cdot R_{\text{DATA}}}, n = \{2,3,4,.. \}$$

Equation 6. $T_{1,n}$ when MDMCFG2.MOD_FORMAT = ASK/OOK

5.2.4 Calculation of T_2

Maximum values for interval T_2 are provided below for different modulation formats. The values for MAX_LNA_GAIN and MAX_DVGA_GAIN are located in the AGCCTRL2 register.

$$T_{\text{GAIN_ADJUST_MAX}} \leq (17.5 - \text{MAX_LNA_GAIN} - \text{MAX_DVGA_GAIN}) \cdot \frac{1}{f_{XOSC}}$$

Equation 7. Variable Time to Adjust Gain

$$T_2 \leq \frac{8 \cdot 2^{\text{AGCCTRL0.FILTER_LENGTH}}}{2 \cdot BW_{\text{channel}}} + T_{\text{GAIN_ADJUST_MAX}}$$

Equation 8. T_2 when MDMCFG2.MOD_FORMAT != ASK/OOK

$$T_2 \leq \frac{9}{8 \cdot R_{\text{DATA}}} + T_{\text{GAIN_ADJUST_MAX}}$$

Equation 9. T_2 when MDMCFG2.MOD_FORMAT = ASK/OOK

When Manchester coding is disabled, the maximum T_2 duration depends on what bits are being transmitted and receiving a series of equal bits can lead to longer maximum T_2 duration than given by Equation 9. However, the maximum time provided for the ASK/OOK T_2 interval holds for all T_2 intervals if Manchester coding is enabled and also when receiving a NRZ 0xAA preamble.

5.2.5 Calculation of RSSI Update Instants/RSSI Response Time

The following equations are referenced to Figure 1 and provide the maximum time in RX for each update instant.

$$RSSI\#1 = T_0 + T_{1,1} + T_2$$

For normal AGC operation ($AGCCTRL0.AGC_FREEZE = \{0, 1, 2\}$) and all modulation formats:

$$RSSI\#(n+1) \leq RSSI\#n + T_{1,n+1} + T_2$$

When $AGCCTRL0.AGC_FREEZE = 1$ and sync is found:

$$RSSI\#(n+1) \leq RSSI\#n + T_2$$

Special case of $AGCCTRL0.AGC_FREEZE = 3$:

MDMCFG2.mod_format != ASK/OOK:

$$RSSI\#(n+1) \leq RSSI\#n + T_2$$

MDMCFG2.mod_format = ASK/OOK:

$$RSSI\#(n+1) \leq RSSI\#n + T_{1,n+1} + T_2$$

5.2.6 Prediction vs. Measurement of RSSI Update Intervals

This section presents predicted (P) and measured (M) results of RSSI update intervals for four different RX configurations, each taken from the SmartRF[®] Studio. Results are given for three different mean RSSI values. The test-setup consisted of two SmartRF04EB boards with one CC1110EM in RX mode and one CC1101EM in TX mode. The CC1101 was configured by SmartRF[®] Studio to send 0xAA preamble, while the measurement results were obtained by configuring a CC1110 to continuously read the `RSSI` register and store both RSSI value and timer1 counter value when a RSSI change occurred. The stored values were then displayed on the LCD. The CC1110 clock frequency was 26 MHz.

Design Note DN505

Configuration				
MOD_FORMAT		0x01	FILTER_LENGTH	0x01
Receiver Filter BW [kHz]		58.035714	WAIT_TIME	0x01
Data Rate [kBaud]		1.19948	DEM_DCFILT_OFF	0x00
AGC_FREEZE		0x00	MAX_LNA_GAIN	0x00
MAX_DVGA_GAIN		0x00		
Results				
RSSI level [dBm]		-86.67	-66.11	-57.78
Type	P(max)	M	M	M
RSSI#1 [us]	1310.3	1309.3	1309.3	1309.3
T1+T2 [us]	276.4	275.4	274.8 - 275.4	274.8 - 275.4
T2 [us]	138.5	137.0 - 137.5	137.0 - 137.5	137.0 - 137.5
# of Gain Updates	N/A	2	3	4
RSSI Response Time [us]	N/A	1584.7	1859.5	2134.4
P(max) = Predicted maximum value, M = Measured value				

Table 2. RSSI Prediction vs. Measurements #1

Configuration				
MOD_FORMAT		0x01	FILTER_LENGTH	0x01
Receiver Filter BW [kHz]		101.5625	WAIT_TIME	0x01
Data Rate [kBaud]		38.3835	DEM_DCFILT_OFF	0x00
AGC_FREEZE		0x00	MAX_LNA_GAIN	0x00
MAX_DVGA_GAIN		0x01		
Results				
RSSI level [dBm]		-86.33	-68.67	-59.33
Type	P(max)	M	M	M
RSSI#1 [us]	291.2	290.0	290.0	290.0
T1+T2 [us]	158.2	156.9	156.9	156.9
T2 [us]	79.4	77.7 - 78.3	77.7 - 78.3	77.7 - 78.3
# of Gain Updates	N/A	2	2	4
RSSI Response Time [us]	N/A	446.9	446.9	760.8
P(max) = Predicted maximum value, M = Measured value				

Table 3. RSSI Prediction vs. Measurements #2

Configuration				
MOD_FORMAT		0x01	FILTER_LENGTH	0x01
Receiver Filter BW [kHz]		101.5625	WAIT_TIME	0x01
Data Rate [kBaud]		38.3835	DEM_DCFILT_OFF	0x01
AGC_FREEZE		0x00	MAX_LNA_GAIN	0x00
MAX_DVGA_GAIN		0x01		
Results				
RSSI level [dBm]		-90.22	-71.33	-61.11
Type	P(max)	M	M	M
RSSI#1 [us]	256.7	256.1	255.5	255.5
T1+T2 [us]	158.2	Not recorded	156.9	156.9
T2 [us]	79.4	77.7 - 78.3	78.3	78.3
# of Gain Updates	N/A	1	3	3
RSSI Response Time [us]	N/A	256.1	569.4	569.4
P(max) = Predicted maximum value, M = Measured value				

Table 4. RSSI Prediction vs. Measurements #3

Design Note DN505

Configuration				
MOD_FORMAT		0x01	FILTER_LENGTH	0x00
Receiver Filter BW [kHz]		541.666667	WAIT_TIME	0x03
Data Rate [kBaud]		249.939	DEM_DCFILT_OFF	0x00
AGC_FREEZE		0x00	MAX_LNA_GAIN	0x00
MAX_DVGA_GAIN		0x03		
Results				
RSSI level [dBm]		-77.57	-44.86	-37.83
Type	P(max)	M	M	M
RSSI#1 [us]	94.8	94.0	93.5	93.5
T1+T2 [us]	37.5	36.3	36.3	36.3
T2 [us]	7.9	6.7 - 7.2	6.7 - 7.2	6.7 - 7.2
# of Gain Updates	N/A	3	3	3
RSSI Response Time [us]	N/A	166.6	166.1	166.1
P(max) = Predicted maximum value, M = Measured value				

Table 5. RSSI Prediction vs. Measurements #4

The results given in Table 2 to Table 5 show that the measured values are within upper bounds given by the equations.

6 Improving RSSI Readout Accuracy

It is important to be aware that in a real system, the output power from the transmitter and variations in the transmission path will contribute to the RSSI inaccuracy. However, there are certain steps one can do, to improve the RSSI readout accuracy

- 1) Calculate an average RSSI value based on several readouts
- 2) Follow workaround for the SPI read synchronization issue (see [5], [6], [7], and [8]). This is only necessary on the CC1100/CC1101/CC1100E/CC2500, not the SoCs.

7 RSSI Threshold

Table 6 shows typical RSSI value at CS threshold when the data rate is 250 kBaud, AGCCTRL2.MAGN_TARGET = 3, and AGCCTRL1.CARRIER_SENSE_ABS_THR = 0.

		AGCCTRL2.MAX_DVGA_GAIN[1:0]			
		00	01	10	11
AGCCTRL2.MAX_LNA_GAIN[2:0]	000	-96	-90	-84	-78.5
	001	-94.5	-89	-83	-77.5
	010	-92.5	-87	-81	-75
	011	-91	-85	-78.5	-73
	100	-87.5	-82	-76	-70
	101	-85	-79.5	-73.5	-67.5
	110	-83	-76.5	-70.5	-65
	111	-78	-72	-66	-60

Table 6. Typical RSSI Value in dBm at CS Threshold

Assume MAX_LNA_GAIN = 4 and MAX_DVGA_GAIN = 1. This means that when MAGN_TARGET = 3 and CARRIER_SENSE_ABS_THR = 0, the RSSI value at CS threshold is -82 dBm.

AGCCTRL2.MAGN_TARGET[2:0]	AGCCTRL1.CARRIER_SENSE_ABS_THR[3:0]
0 24 dBm	-8 Absolute carrier sense threshold disabled
1 27 dBm	-7 7 dB below MAGN_TARGET setting
2 30 dBm
3 33 dBm	-1 1 dB below MAGN_TARGET setting
4 36 dBm	0 At MAGN_TARGET setting
5 38 dBm	1 1 dB above MAGN_TARGET setting
6 40 dBm
7 42 dBm	7 7 dB above MAGN_TARGET setting

Table 7. MAGN_TARGET and CARRIER_SENSE_ABS_THR Settings

Changing MAGN_TARGET to 7 and CARRIER_SENSE_ABS_THR to 4, will change the CS threshold from -82 dBm to -69 dBm ($-82 + (42 - 33) + (4 - 0) = -69$ [dBm]).

8 References

- [1] CC1100 Single-Chip Low Cost Low Power RF-Transceiver, Data sheet (cc1100.pdf)
- [2] CC1101 Single-Chip Low Cost Low Power RF-Transceiver, Data sheet (cc1101.pdf)
- [3] CC2500 Single-Chip Low Cost Low Power RF-Transceiver, Data sheet (cc2500.pdf)
- [4] CC1100E Single-Chip Low Cost Low Power RF-Transceiver, Data sheet (cc1100E.pdf)
- [5] CC1100 Errata Notes (swrz012.pdf)
- [6] CC1101 Errata Notes (swrz020.pdf)
- [7] CC2500 Errata Notes (swrz002.pdf)
- [8] CC1100E Errata Notes (swrz029.pdf)
- [9] CC430 User's Guide (slau259.pdf)
- [10] CC1110Fx/CC1111Fx Low-Power Sub-1 GHz RF System-on-Chip (SoC) with MCU, Memory, Transceiver, and USB Controller (cc1110f32.pdf)
- [11] CC2510Fx/CC2511Fx Low-Power SoC (System-on-Chip) with MCU, Memory, 2.4 GHz RF Transceiver, and USB Controller (cc2510f32.pdf)

9 General Information

9.1 Document History

Revision	Date	Description/Changes
SWRA114D	2010.06.15	More detailed information about RSSI response time. Equations used to estimate response time has been changed.
SWRA114C	2009.03.12	Added info about CC1100E. Added info to Table 1.
SWRA114B	2007.10.22	Removed logo from header. Added info about CC1101 and CC1111. Added info to Table 1.
SWRA114A	2007.01.12	Corrected error in code example. Added chapter 7. RSSI Threshold
SWRA114	2006.10.23	Initial release.

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