

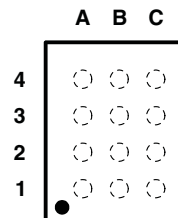
4-BIT BIDIRECTIONAL VOLTAGE-LEVEL TRANSLATOR FOR OPEN-DRAIN AND PUSH-PULL APPLICATIONS

FEATURES

- No Direction-Control Signal Needed
- Max Data Rates
 - 24 Mbps (Push Pull)
 - 2 Mbps (Open Drain)
- Available in the Texas Instruments NanoFree™ Package
- 1.65 V to 3.6 V on A port and 2.3 V to 5.5 V on B port ($V_{CCA} \leq V_{CCB}$)
- No Power-Supply Sequencing Required – V_{CCA} or V_{CCB} Can Be Ramped First
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - A Port
 - 2000-V Human-Body Model (A114-B)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
 - B Port
 - 15-kV Human-Body Model (A114-B)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

- IEC 61000-4-2 ESD (B Port)
 - ±8-kV Contact Discharge
 - ±10-kV Air-Gap Discharge

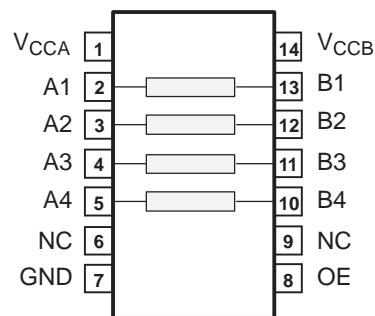
**GXU/ZXU (BGA) PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS
(GXU/ZXU Package)**

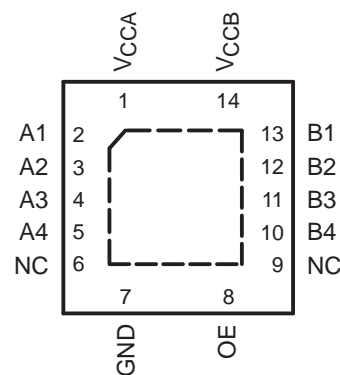
	A	B	C
4	A4	GND	B4
3	A3	OE	B3
2	A2	V_{CCA}	B2
1	A1	V_{CCB}	B1

**D OR PW PACKAGE
(TOP VIEW)**



NC – No internal connection

**RGY PACKAGE
(TOP VIEW)**



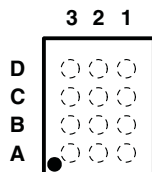
NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

**YZT (WCSP) PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS
(YZT Package)**

	3	2	1
D	A4	GND	B4
C	A3	OE	B3
B	A2	V _{CCA}	B2
A	A1	V _{CCB}	B1

DESCRIPTION/ORDERING INFORMATION

This 4-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.65 V to 3.6 V. V_{CCA} must be less than or equal to V_{CCB}. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 2.3 V to 5.5 V. This allows for low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

The TXS0104E is designed so that the OE input circuit is supplied by V_{CCA}.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION

T _A	PACKAGE ⁽¹⁾⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	NanoFree — WCSP (DSBGA) 0.23-mm Large Bump – YZT (Pb-free) 0.625-mm max height	Reel of 3000	TXS0104EYZTR	2N7
	UFBGA – GXU	Reel of 2500	TXS0104EGXUR	YF04E
	UFBGA – ZXU (Pb-free)		TXS0104EZKUR	
	QFN – RGY	Reel of 1000	TXS0104ERGYR TXS0104ERGYRG4	YF04E
	SOIC – D	Tube of 50	TXS0104ED TXS0104EDG4	TXS0104E
			Reel of 2500	
		TSSOP – PW	Reel of 2000	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) YZT: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

PIN DESCRIPTION

PIN NO.	BALL NO.		NAME	FUNCTION
	GXU/ZXU	YZT		
1	B2	B2	V _{CCA}	A-port supply voltage. $1.65\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$ and $V_{CCA} \leq V_{CCB}$.
2	A1	A3	A1	Input/output A1. Referenced to V _{CCA} .
3	A2	B3	A2	Input/output A2. Referenced to V _{CCA} .
4	A3	C3	A3	Input/output A3. Referenced to V _{CCA} .
5	A4	D3	A4	Input/output A4. Referenced to V _{CCA} .
6	–	–	NC	No connection. Not internally connected.
7	B4	D2	GND	Ground
8	B3	C2	OE	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V _{CCA} .
9	–	–	NC	No connection. Not internally connected.
10	C4	D1	B4	Input/output B4. Referenced to V _{CCB} .
11	C3	C1	B3	Input/output B3. Referenced to V _{CCB} .
12	C2	B1	B2	Input/output B2. Referenced to V _{CCB} .
13	C1	A1	B1	Input/output B1. Referenced to V _{CCB} .
14	B1	A2	V _{CCB}	B-port supply voltage. $2.3\text{ V} \leq V_{CCB} \leq 5.5\text{ V}$.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V _{CCA}	Supply voltage range	–0.5	4.6	V	
V _{CCB}		–0.5	6.5		
V _I	Input voltage range ⁽²⁾	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	A port	–0.5	4.6	V
		B port	–0.5	6.5	
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	A port	–0.5	V _{CCA} + 0.5	V
		B port	–0.5	V _{CCB} + 0.5	
I _{IK}	Input clamp current	V _I < 0	–50	mA	
I _{OK}	Output clamp current	V _O < 0	–50	mA	
I _O	Continuous output current		±50	mA	
	Continuous current through each V _{CCA} , V _{CCB} , or GND		±100	mA	
θ _{JA}	Package thermal impedance	D package ⁽⁴⁾		86	°C/W
		PW package ⁽⁴⁾		113	
		RGY package ⁽⁵⁾		47	
		GXU/ZXU package ⁽⁴⁾		128	
		YZT package		TBD	
T _{stg}	Storage temperature range	–65	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

(5) The package thermal impedance is calculated in accordance with JESD 51-5.

Recommended Operating Conditions⁽¹⁾⁽²⁾

		V_{CCA}	V_{CCB}	MIN	MAX	UNIT	
V_{CCA}	Supply voltage ⁽³⁾			1.65	3.6	V	
V_{CCB}				2.3	5.5		
V_{IH}	High-level input voltage	A-port I/Os	2.3 V to 5.5 V	1.65 V to 1.95 V	$V_{CCI} - 0.2$	V_{CCI}	
				2.3 V to 3.6 V	$V_{CCI} - 0.4$	V_{CCI}	
		B-port I/Os	2.3 V to 5.5 V	1.65 V to 3.6 V	$V_{CCI} - 0.4$	V_{CCI}	
OE input		$V_{CCA} \times 0.65$		5.5			
V_{IL}	Low-level input voltage	A-port I/Os	2.3 V to 5.5 V	0	0.15	V	
		B-port I/Os		1.65 V to 3.6 V	0		0.15
		OE input			0		$V_{CCA} \times 0.35$
$\Delta t/\Delta v$	Input transition rise or fall rate	A-port I/Os, push-pull driving	2.3 V to 5.5 V		10	ns/V	
		B-port I/Os, push-pull driving		1.65 V to 3.6 V			10
		Control input					10
T_A	Operating free-air temperature			-40	85	°C	

- (1) V_{CCI} is the supply voltage associated with the input port.
(2) V_{CCO} is the supply voltage associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB} , and V_{CCA} must not exceed 3.6 V.

Electrical Characteristics⁽¹⁾⁽²⁾⁽³⁾

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CCA}	V _{CCB}	T _A = 25°C			T _A = 25°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OHA}	I _{OH} = -20 μA, V _{IB} ≥ V _{CCB} - 0.4 V	1.65 V to 3.6 V	2.3 V to 5.5 V				V _{CCA} × 0.8		V
V _{OLA}	I _{OL} = 1 mA, V _{IB} ≤ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V				0.4		V
V _{OHB}	I _{OH} = -20 μA, V _{IA} ≥ V _{CCA} - 0.2 V	1.65 V to 3.6 V	2.3 V to 5.5 V				V _{CCB} × 0.8		V
V _{OLB}	I _{OL} = 1 mA, V _{IA} ≤ 0.15 V	1.65 V to 3.6 V	2.3 V to 5.5 V				0.4		V
I _I	OE	V _I = V _{CCI} or GND	1.65 V to 3.6 V	2.3 V to 5.5 V			±1	±2	μA
I _{OZ}	A or B port	OE = V _{IL}	1.65 V to 3.6 V	2.3 V to 5.5 V			±1	±2	μA
I _{CCA}	V _I = V _O = Open, I _O = 0	1.65 V to V _{CCB}	2.3 V to 5.5 V				2.4		μA
		3.6 V	0				2.2		
		0	5.5 V				-1		
I _{CCB}	V _I = V _O = Open, I _O = 0	1.65 V to V _{CCB}	2.3 V to 5.5 V				12		μA
		3.6 V	0				-1		
		0	5.5 V				1		
I _{CCA} + I _{CCB}	V _I = V _O = Open, I _O = 0	1.65 V to V _{CCB}	2.3 V to 5.5 V				14.4		μA
C _I	OE		3.3 V	3.3 V		2.5	3.5		pF
C _{Io}	A port		3.3 V	3.3 V		5	6.5		pF
	B port					12	16.5		

- (1) V_{CCI} is the supply voltage associated with the input port.
 (2) V_{CCO} is the supply voltage associated with the output port.
 (3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6 V.

Timing Requirements

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted)

		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull driving	24		24		24		Mbps
	Open-drain driving	2		2		2		
t_w Pulse duration	Push-pull driving	41		41		41		ns
	Open-drain driving	500		500		500		

Timing Requirements

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Data rate	Push-pull driving	24		24		24		Mbps
	Open-drain driving	2		2		2		
t_w Pulse duration	Push-pull driving	41		41		41		ns
	Open-drain driving	500		500		500		

Timing Requirements

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
Data rate	Push-pull driving	24		24		Mbps
	Open-drain driving	2		2		
t_w Pulse duration	Push-pull driving	41		41		ns
	Open-drain driving	500		500		

Switching Characteristics

 over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	Push-pull driving	4.6		4.7		5.8		ns
			Open-drain driving	2.9	8.8	2.9	9.6	3	10	
t_{PLH}			Push-pull driving	6.8		6.8		7		
			Open-drain driving	45	260	36	208	27	198	
t_{PHL}	B	A	Push-pull driving	4.4		4.5		4.7		ns
			Open-drain driving	1.9	5.3	1.1	4.4	1.2	4	
t_{PLH}			Push-pull driving	5.3		4.5		0.5		
			Open-drain driving	45	175	36	140	27	102	
t_{en}	OE	A or B		200		200		200		ns
t_{dis}	OE	A or B		50		40		35		ns
t_{rA}	A-port rise time		Push-pull driving	3.2	9.5	2.3	9.3	2	7.6	ns
			Open-drain driving	38	165	30	132	22	95	
t_{rB}	B-port rise time		Push-pull driving	4	10.8	2.7	9.1	2.7	7.6	ns
			Open-drain driving	34	145	23	106	10	58	
t_{fA}	A-port fall time		Push-pull driving	2	5.9	1.9	6	1.7	13.3	ns
			Open-drain driving	4.4	6.9	4.3	6.4	4.2	6.1	
t_{fB}	B-port fall time		Push-pull driving	2.9	7.6	2.8	7.5	2.8	8.8	ns
			Open-drain driving	6.9	13.8	7.5	16.2	7	16.2	
$t_{SK(O)}$	Channel-to-channel skew			1		1		1		ns
Max data rate			Push-pull driving	24		24		24		Mbps
			Open-drain driving	2		2		2		

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	A	B	Push-pull driving	3.2		3.3		3.4		ns
			Open-drain driving	1.7	6.3	2	6	2.1	5.8	
t_{PLH}			Push-pull driving	3.5		4.1		4.4		
			Open-drain driving	43	250	36	206	27	190	
t_{PHL}	B	A	Push-pull driving	3		3.6		4.3		ns
			Open-drain driving	1.8	4.7	2.6	4.2	1.2	4	
t_{PLH}			Push-pull driving	2.5		1.6		0.7		
			Open-drain driving	44	170	37	140	27	103	
t_{en}	OE	A or B		200		200		200		ns
t_{dis}	OE	A or B		50		40		35		ns
t_{rA}	A-port rise time		Push-pull driving	2.8	7.4	2.6	6.6	1.8	5.6	ns
			Open-drain driving	34	149	28	121	24	89	
t_{rB}	B-port rise time		Push-pull driving	3.2	8.3	2.9	7.2	2.4	6.1	ns
			Open-drain driving	35	151	24	112	12	64	
t_{fA}	A-port fall time		Push-pull driving	1.9	5.7	1.9	5.5	1.8	5.3	ns
			Open-drain driving	4.4	6.9	4.3	6.2	4.2	5.8	
t_{fB}	B-port fall time		Push-pull driving	2.2	7.8	2.4	6.7	2.6	6.6	ns
			Open-drain driving	5.1	8.8	5.4	9.4	5.4	10.4	
$t_{SK(O)}$	Channel-to-channel skew			1		1		1		ns
Max data rate			Push-pull driving	24		24		24		Mbps
			Open-drain driving	2		2		2		

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
				MIN	MAX	MIN	MAX	
t_{PHL}	A	B	Push-pull driving	2.4		3.1		ns
t_{PLH}			Open-drain driving	1.3	4.2	1.4	4.6	
			Push-pull driving	4.2		4.4		
Open-drain driving			36	204	28	165		
t_{PHL}	B	A	Push-pull driving	2.5		3.3		ns
t_{PLH}			Open-drain driving	1	124	1	97	
			Push-pull driving	2.5		2.6		
Open-drain driving			3	139	3	105		
t_{en}	OE	A or B		200		200		ns
t_{dis}	OE	A or B		40		35		ns
t_{rA}	A-port rise time		Push-pull driving	2.3	5.6	1.9	4.8	ns
			Open-drain driving	25	116	19	85	
t_{rB}	B-port rise time		Push-pull driving	2.5	6.4	2.1	7.4	ns
			Open-drain driving	26	116	14	72	
t_{fA}	A-port fall time		Push-pull driving	2	5.4	1.9	5	ns
			Open-drain driving	4.3	6.1	4.2	5.7	
t_{fB}	B-port fall time		Push-pull driving	2.3	7.4	2.4	7.6	ns
			Open-drain driving	5	7.6	4.8	8.3	
$t_{SK(O)}$	Channel-to-channel skew			1		1		ns
Max data rate			Push-pull driving	24		24		Mbps
			Open-drain driving	2		2		

PRINCIPLES OF OPERATION

Applications

The TXS0104E can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXS0104E is ideal for use in applications where an open-drain driver is connected to the data I/Os. The TXS0104E can also be used in applications where a push-pull driver is connected to the data I/Os, but the TXB0104 might be a better option for such push-pull applications.

Architecture

The TXS0104E architecture (see [Figure 1](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A.

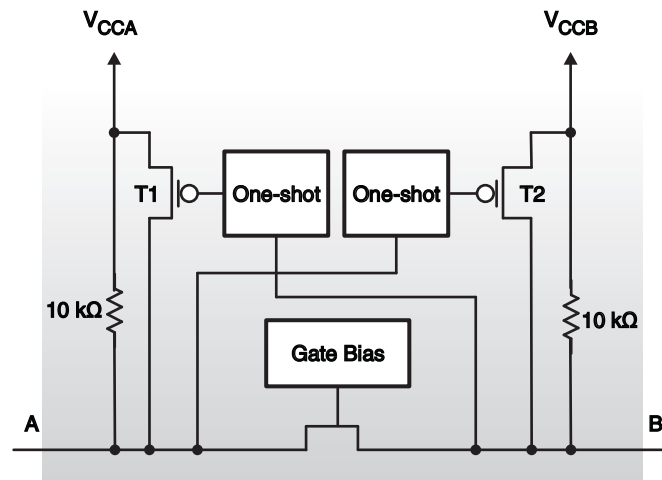


Figure 1. Architecture of a TXS01xx Cell

Each A-port I/O has an internal 10-k Ω pullup resistor to V_{CCA} , and each B-port I/O has an internal 10-k Ω pullup resistor to V_{CCB} . The output one-shots detect rising edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1,T2) for a short duration, which speeds up the low-to-high transition.

Input Driver Requirements

The fall time (t_{fA} , t_{fB}) of a signal depends on the output impedance of the external device driving the data I/Os of the TXS0104E. Similarly, the t_{PHL} and max data rates also depend on the output impedance of the external driver. The values for t_{fA} , t_{fB} , t_{PHL} , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50 Ω .

Power Up

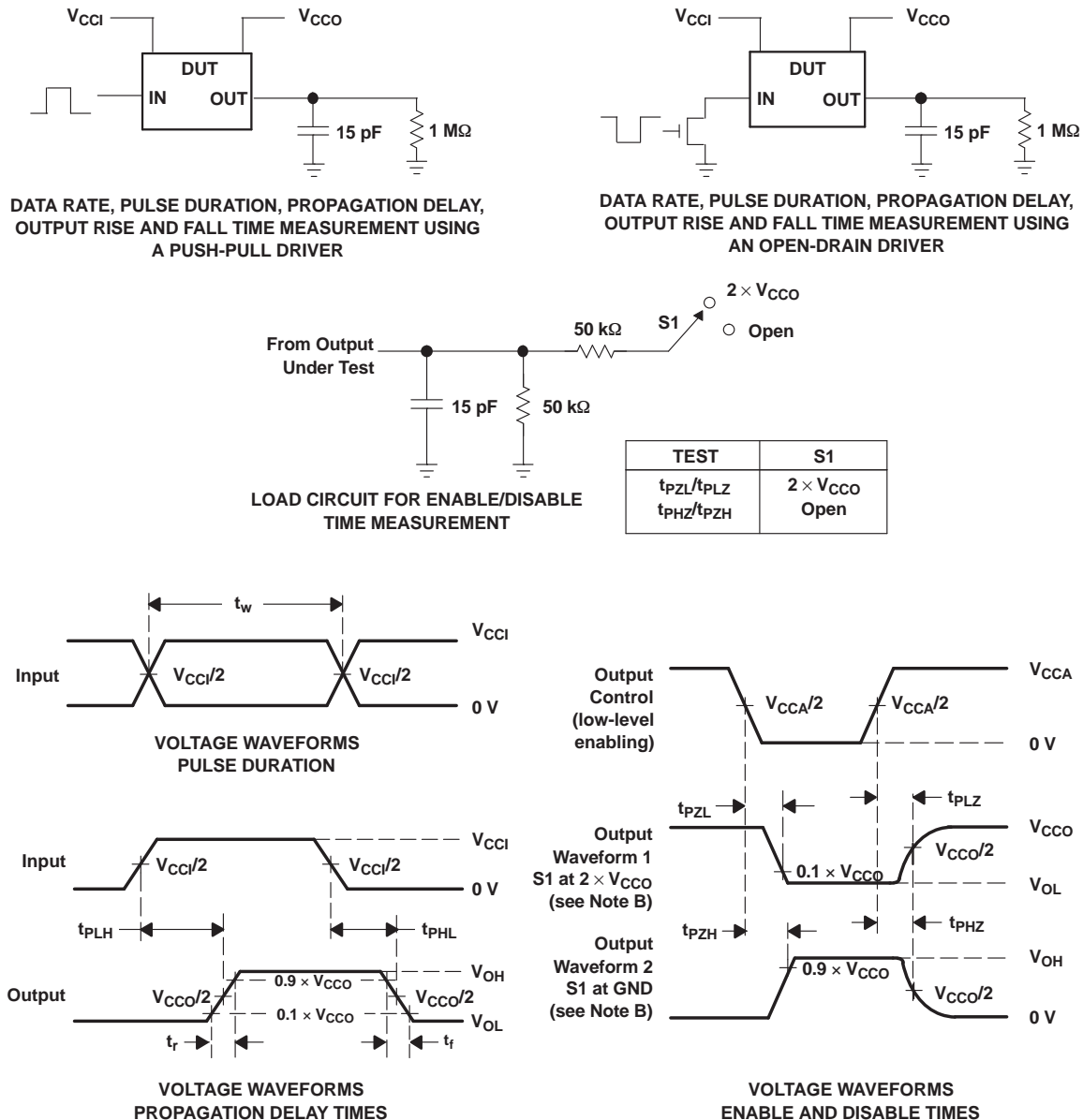
During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. During power-up sequencing, $V_{CCA} \geq V_{CCB}$ does not damage the device, so any power supply can be ramped up first.

Enable and Disable

The TXS0104E has an OE input that is used to disable the device by setting OE low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken high.

Pullup or Pulldown Resistors on I/O Lines

Each A-port I/O has an internal 10-k Ω pullup resistor to V_{CCA} , and each B-port I/O has an internal 10-k Ω pullup resistor to V_{CCB} . If a smaller value of pullup resistor is required, an external resistor must be added from the I/O to V_{CCA} or V_{CCB} (in parallel with the internal 10-k Ω resistors).

PARAMETER MEASUREMENT INFORMATION


- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- F. t_{PZL} and t_{PZH} are the same as t_{en} .
- G. t_{PLH} and t_{PHL} are the same as t_{pd} .
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
TXS0104ED	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
TXS0104EDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Contact TI Distributor or Sales Office
TXS0104EDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TXS0104EDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TXS0104EGXUR	ACTIVE	BGA MICROSTAR JUNIOR	GXU	12	2500	TBD	SNPB	Level-1-240C-UNLIM	Purchase Samples
TXS0104EPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TXS0104EPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TXS0104ERGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
TXS0104ERGYRG4	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
TXS0104EYZTR	ACTIVE	DSBGA	YZT	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples
TXS0104EZXR	ACTIVE	BGA MICROSTAR JUNIOR	ZXU	12	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0104EDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TXS0104EGXUR	BGA MICROSTAR JUNIOR	GXU	12	2500	330.0	8.4	2.3	2.8	1.0	4.0	8.0	Q2
TXS0104EPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TXS0104ERGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
TXS0104EYZTR	DSBGA	YZT	12	3000	180.0	8.4	1.49	1.99	0.75	4.0	8.0	Q2
TXS0104EZXR	BGA MICROSTAR JUNIOR	ZXU	12	2500	330.0	8.4	2.3	2.8	1.0	4.0	8.0	Q2

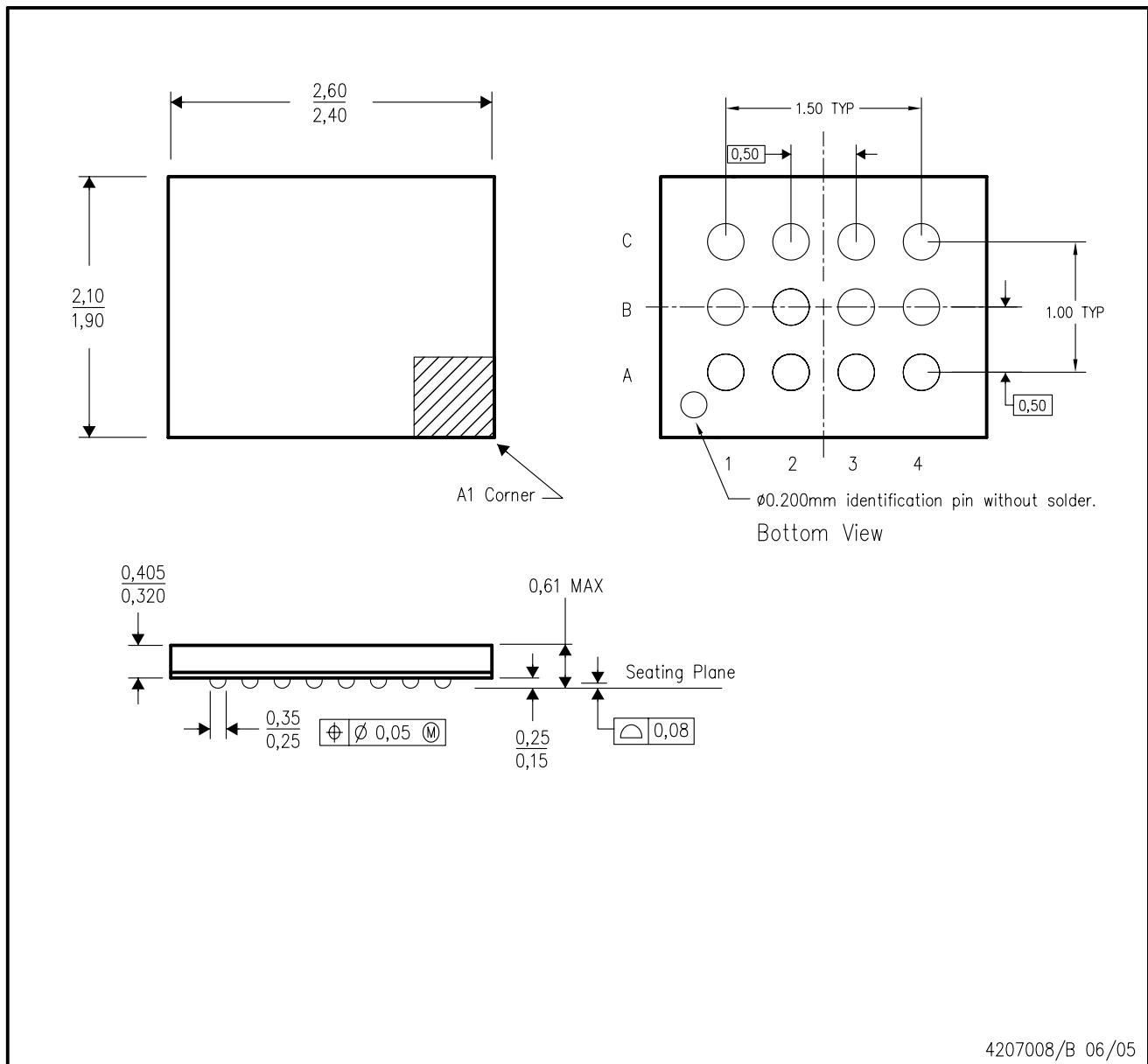
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0104EDR	SOIC	D	14	2500	346.0	346.0	33.0
TXS0104EGXUR	BGA MICROSTAR JUNIOR	GXU	12	2500	340.5	338.1	20.6
TXS0104EPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
TXS0104ERGYR	VQFN	RGY	14	3000	346.0	346.0	29.0
TXS0104EYZTR	DSBGA	YZT	12	3000	210.0	185.0	35.0
TXS0104EZXR	BGA MICROSTAR JUNIOR	ZXU	12	2500	340.5	338.1	20.6

GXU (S-PBGA-N12)

PLASTIC BALL GRID ARRAY

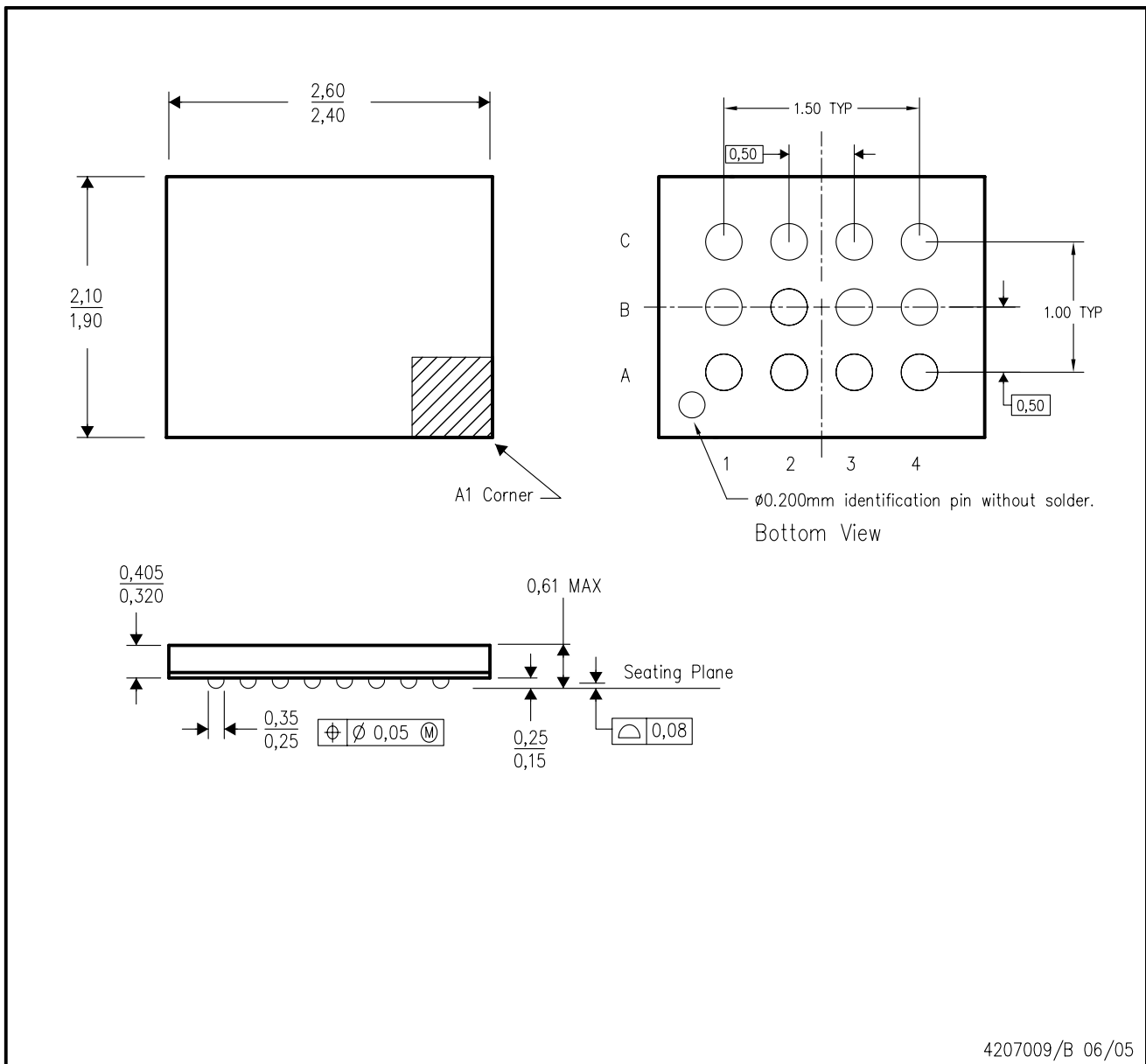


4207008/B 06/05

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.

ZXU (S-PBGA-N12)

PLASTIC BALL GRID ARRAY



4207009/B 06/05

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. This package is a lead-free solder ball design.

D (R-PDSO-G14)

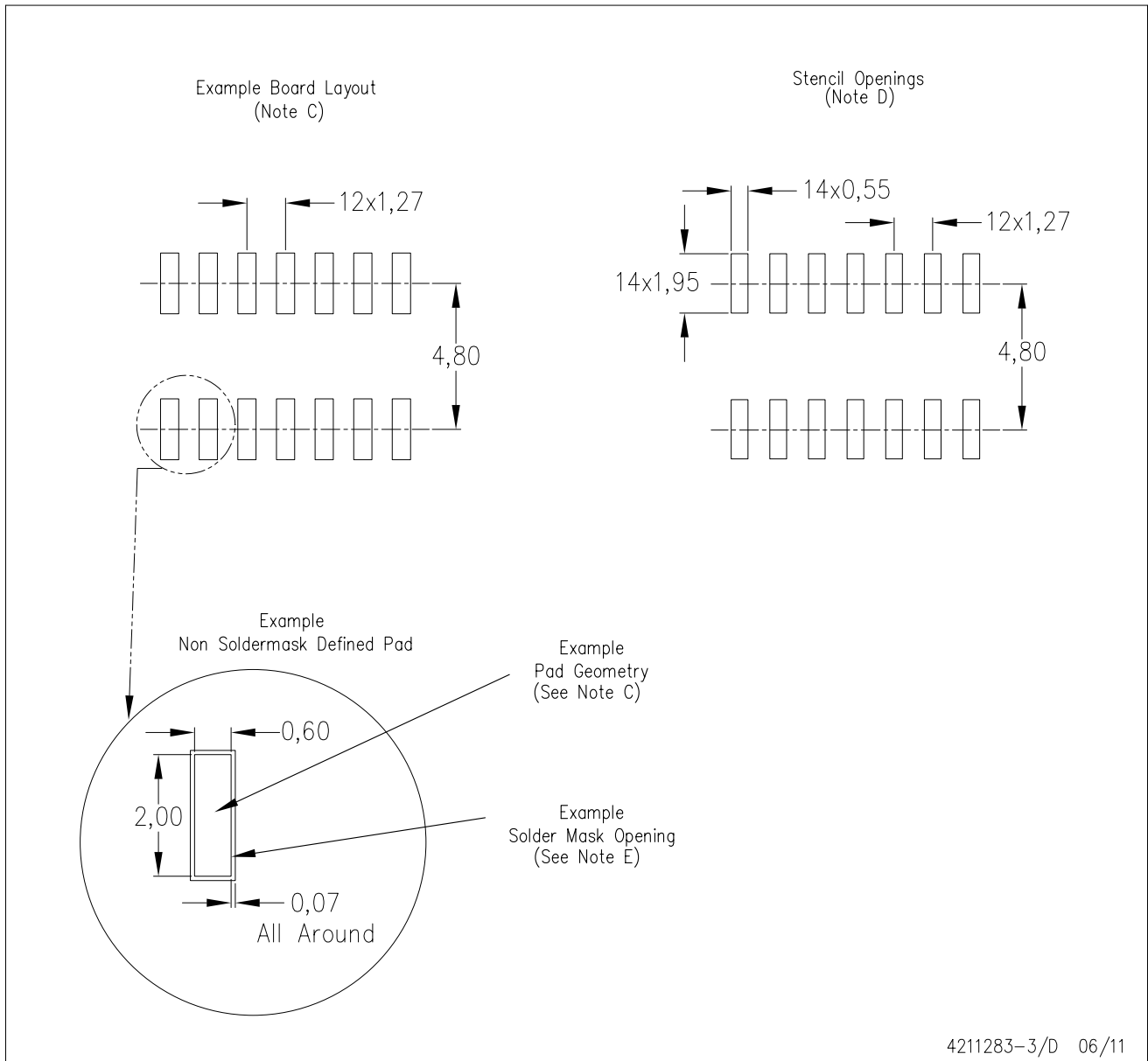
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

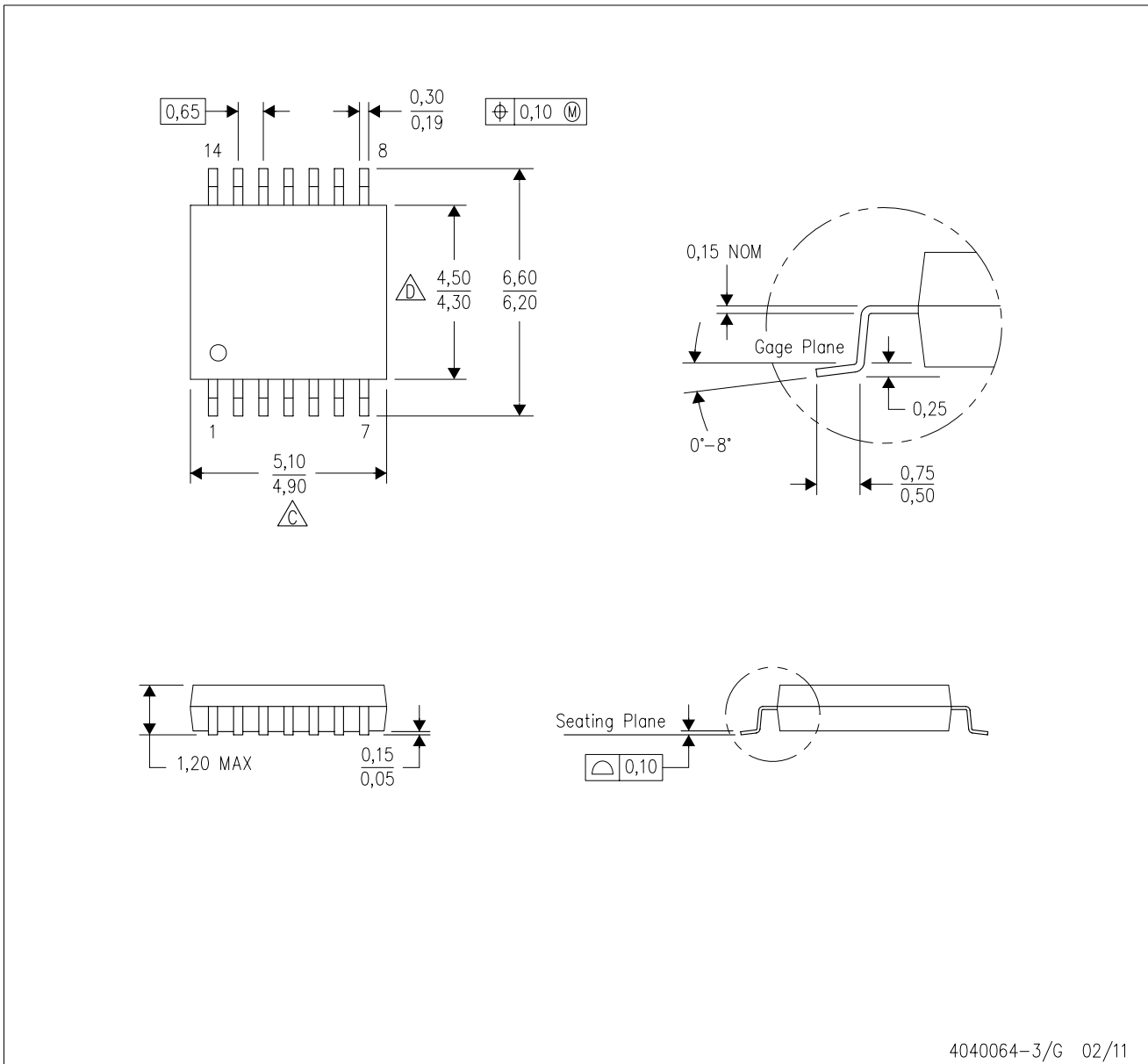
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

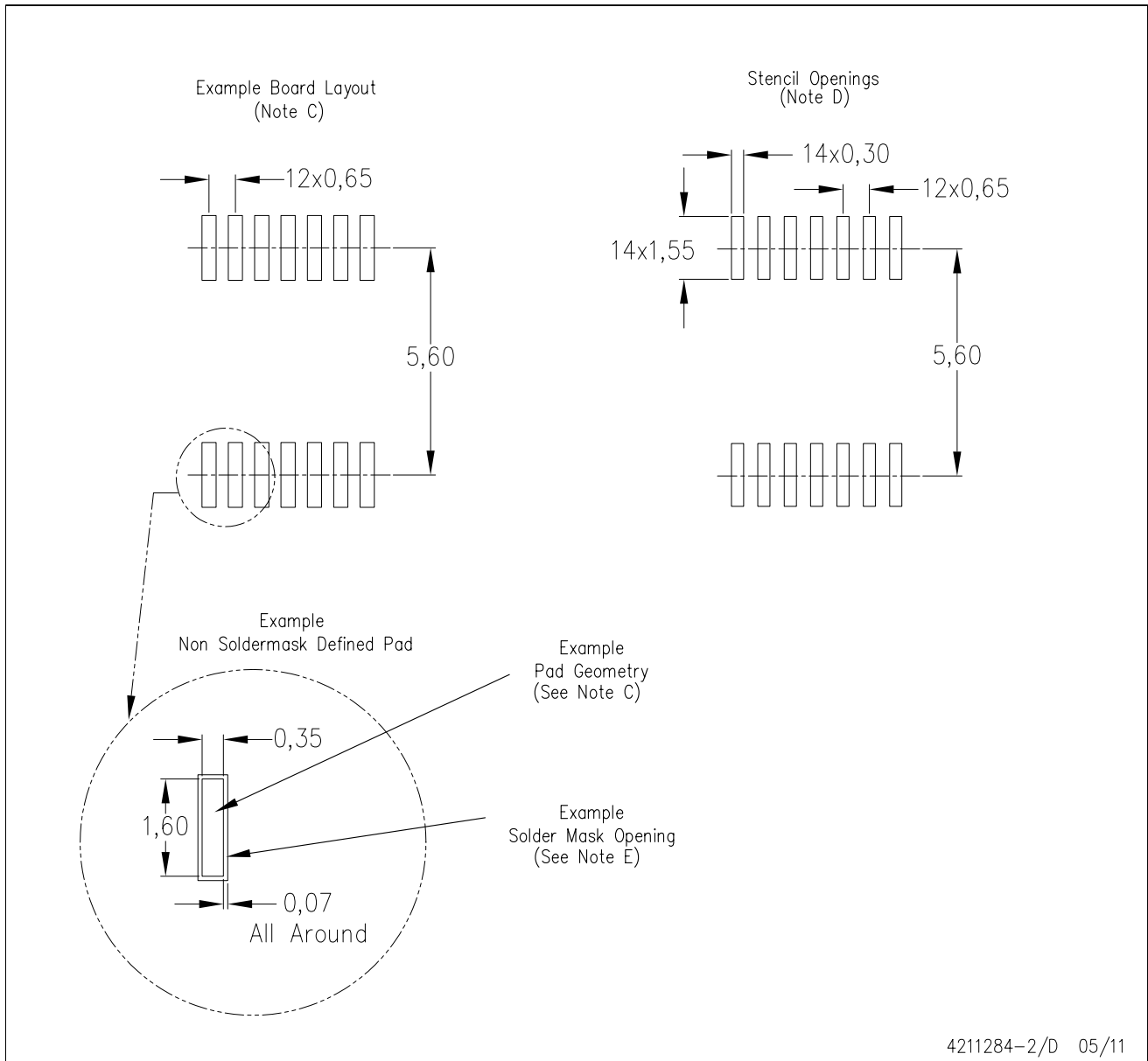


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/0 11/11

NOTE: All linear dimensions are in millimeters

RGY (S-PVQFN-N14)

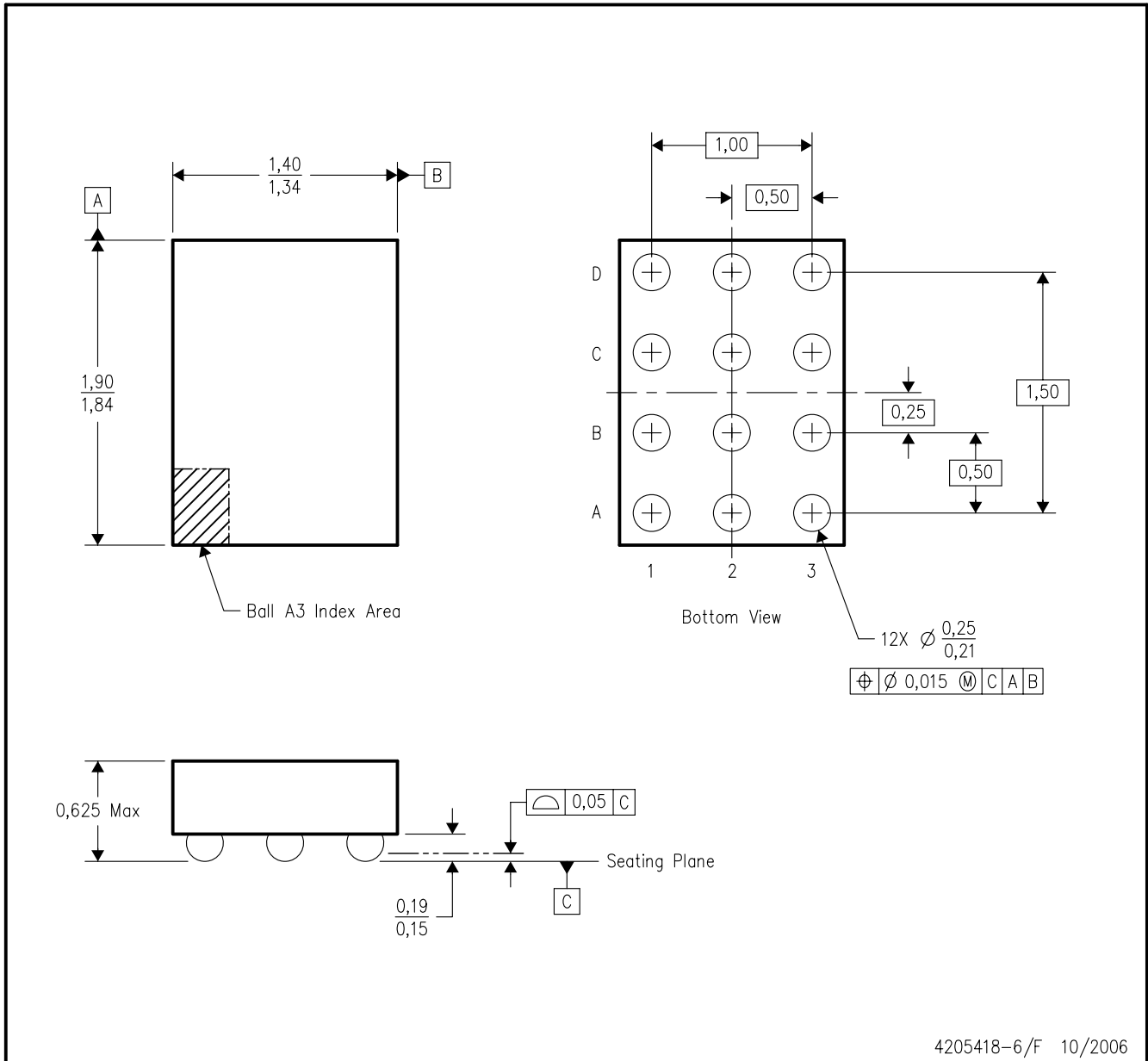
PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YZT (R-XBGA-N12)

(CUSTOM) DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This is a lead-free solder ball design.

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