

Up till now some mistakes seen are:

1. VBAT left unconnected.

It must not be left unconnected, or it will not work correctly. It must not be left open, as it still powers a portion of the internal circuitry. If you do not care cold starting each time powering up, connect VBAT to 3.3V as pin-2; otherwise connect to some backup supply voltage (battery device) so that even after main power is removed, there will still be supply voltage to keep the internal RTC running and SRAM data retained, such that if powering up again within 2 hours then it'll get position fix quickly within a couple seconds without having to download ephemeris again (18~30second under open sky).

2. Pin-9 left open or connect to GND directly.

Venus634FLPx pin-9 needs a pull-down resistor; grounding Venus634FLPx pin-9 directly to GND will render the chip not working. For Venus634FLPx, pin-9 is actually address bus bit16 output from the CPU to the Flash memory. During boot up, it is changed into input mode to select booting from ROM or Flash. After the initial bootup reset period, the pin later functions as CPU address output pin. That is why a pull-down resistor is needed at pin-9, to select booting from Flash memory but not to short the address bus bit16 to ground. If leaving pin-9 open, internal ROM mode is selected; although it is older version firmware, it still works reasonably well.

Pin-9 is unconnected to anything internally with Venus634LPx. To make the design changeable for both Venus634LPx and Venus634FLPx, use a pull-down resistor for pin-9 even for Venus634LPx design.

3. R/C delay circuit omitted on pin-1.

The internal reset cell only has 3~5usec duration. For fast rise time 3.3V supply input, it may not be needed. For slow supply, it stretches the reset pulse longer so that internal CPU can be properly reset after supply voltage ramp up to 3V. For supply voltage with very slow rise time, even the R/C reset stretcher delay circuit will fail, then reset IC with longer reset period is needed. We recommend at least a R/C delay network to pin-1.

4. RF ground and system ground tied together

For best performance, the RF grounds should be tied together by an independent ground plane on the component side. The digital system grounds can be connected to the application system ground plane. The digital system ground and RF ground is tied together through a single point within the chip, thus there is no need to connect the RF ground plane to the system ground on the PCB.

Although we have the 2 ground planes connected together within our chip, we showed

using a 0-ohm resistor for connecting the two grounds in the reference schematic, to prevent inadvertently electrically shortening of active antenna connection blowing open the thin connecting line trace within the chip for the high return ground current.